KNOWLEDGE PROBE 2: Phase-Locked Loops
Phase-Locked Loop Applications

Learning Objectives

1. Describe the operation of the PLL as a filter.
2. Describe the operation of the PLL as a clock and data recovery circuit.
3. Describe the operation of the PLL as an FM demodulator.
4. Describe the operation of the PLL as a clock multiplier.
5. Describe the operation of the PLL as a frequency synthesizer.

1. The bandwidth of a band pass filter implemented with a PLL is set by?
   a. The capture range
   b. The loop filter characteristics
   c. Both of the above
   d. None of the above

2. A PLL BPF is useful in minimizing noise on an input signal?
   a. True
   b. False

3. The output of a PLL band pass filter is an attenuated or amplified version of the input signal?
   a. True
   b. False

4. The name for the precise timing signal used in most digital circuits and computer is the?
   a. Clock
   b. Multivibrator
   c. Oscillator
   d. Quartz crystal

5. The PLL circuit that rejuvenates a noisy and distorted clock signal is a?
   a. Band pass filter
   b. Clock and data recovery circuit
   c. Clock oscillator
   d. Frequency synthesizer

6. A PLL CDR can extract the clock from a data signal?
   a. True
   b. False

7. The output of a PLL is usually from the?
   a. Frequency divider
   b. Loop filter
   c. Phase detector
   d. VCO

8. The output of a PLL used as a frequency demodulator is taken from the?
   a. Frequency divider
   b. Loop filter
   c. Phase detector
   d. VCO

9. The main difference between a standard PLL and a clock multiplier PLL is that the latter contains a?
   a. Frequency divider
   b. Mixer
   c. Multiplying circuit
   d. Second loop filter

10. A 13.56 MHz crystal oscillator is connected to the input of a PLL with a frequency divider with a divide factor of 67. The VCO output is?
    a. 202.388 kHz
    b. 433.92 MHz
    c. 705.12 MHz
    a. 908.52 MHz

11. Clock multipliers are useful because?
    a. They are more stable than a crystal oscillator
    b. They can generate multiple frequencies
    c. They can produce output frequencies at higher frequencies
    a. They can replace conventional clock oscillators

12. Which of the following does NOT contain a PLL frequency synthesizer?
    a. Cable box
    b. Cell phone
    c. Guitar amplifier
    a. TV set

13. Which of the following is NOT true about a frequency synthesizer?
    a. It generates a sine or rectangular output signal
    b. It uses a crystal oscillator input to set the stability
    c. The Frequency output varies continuously
    a. The frequency output varies in increments

14. Calculate the output frequency of a PLL synthesizer with a 25 kHz input and a divide ratio of 2048?
    a. 5.12 MHz
    b. 12.5 MHz
    c. 51.2 MHz
    a. 81.92 MHz

15. How is the output frequency of a PLL synthesizer changed?
    a. Manual input to the divider from a switch
    b. Output from a control microprocessor
    c. Parallel input of a binary number to the divider
    d. Serial input of the binary number to the divider
    e. Any of the above

16. A PLL synthesizer has a crystal reference oscillator of 50 MHz followed by frequency divider of N = 100 whose output drives the phase detector input. The VCO output changes in increments of?
    a. 100 Hz
    b. 500 kHz
    c. 5 MHz
    a. 50 MHz

17. The circuit that reduces the VCO output frequency so that it is within range of the frequency divider is called a?
    a. Down counter
    b. Flip flop
    c. Prescaler
    a. Shift register

18. A fractionalN PLL synthesizer has A = 20, M = 32, and N = 150. The reference input frequency is 1 MHz. What is the VCO output frequency?
    a. 245 MHz
    b. 54.6 MHz
    c. 122 MHz
    a. 4.82 GHz

19. A mixer has inputs of 590 kHz and 1.045 MHz. The difference output is?
    a. 455 kHz
    b. 590 kHz
    c. 780 kHz
    e. 1635 kHz

20. A mixer used to translate an input signal to a higher frequency is called a(n)?
    a. Demodulator
    b. Differentiator
    c. Downconverter
    d. Upconverter

21. A common use of a mixer in a PLL synthesizer is to?
    a. Change the divider ratio
    b. Downconvert the VCO output
    c. Set the input reference frequency
    d. Use a lower crystal frequency

22. What does a PLL control in a motor?
    a. Run time
    b. Speed
    c. Torque
    d. Voltage

23. What replaces the VCO in a PLL motor controller?
    a. DC voltage
    b. Divider
    c. Phase detector
    d. Tachometer

24. An input signal that determines the speed of a motor is known as the?
    a. Control frequency
    b. Control voltage
    c. Dead zone
    d. Set point

25. If the load on a motor PLL motor controller is reduced thereby increasing its speed, what does the PLL do?
    a. Adjusts the motor speed to the speed initially determined by the set point
    b. Adjusts the motor to the new higher speed
    c. Nothing
    d. Reduces the speed of the motor