Phase-Locked Loops Circuit Lab

Lab Summary: The purpose of this hands-on laboratory is to construct a phase-locked loop circuit and observe the relationship between in the input frequency and DC output frequency.

Lab Goal: Construct a PLL circuit, observe its operation, and perform measurements related to its operation.

Learning Objectives

1. Construct a circuit using a PLL to gain an understanding of how the PLL functions.
2. Understand, by experimentation, the relationship between the DC output voltage and the input frequency.
3. Measure the lock range of the PLL.

Grading Criteria: Your lab grade is determined by your performance in the lab and answers to the lab questions.

Approximate Time Required: 3 hours

Equipment and Supplies

Part	Quantity	Description
Equipment:		
Protoboard (Breadboard)	1	Circuit assembly board
Audio frequency generator	1	
Oscilloscope, 2 channel, probes	1	Digital storage capability helpful but not required
Hookup wire		
Wire stripping tool		
Frequency counter	1	
Power supply	1	1 ±10v DC output
VOM or DMM	1	
Components:		
PLL: NE565	1	
Potentiometer	1	1 kΩ
½ W Resistor	1	1 kΩ,
½ W Resistor	2	2.2 kΩ
Capacitors	1	0.047 µF
Capacitors	2	0.1 µF
Capacitors	2	0.47 µF
Capacitors	1	1.0 µF

Lab Preparation

1. Read web based WRE "Phase-Locked Loops".
2. Print this entire procedure to use as a reference, schematic, and workbook while completing the lab.
3. Read the Introduction (below).
4. Review the Lab Procedures (below).

Introduction

The phase-locked loop (PLL) is a feedback system that contains a phase detector, low-pass filter, and a voltage controlled oscillator (VCO). The phase detector compares two input signals and produces an output. The inputs to the phase detector are the external signal used in the application and the VCO output. The low pass filter smoothes the phase detector output into a DC voltage that is used to control the VCO frequency. The VCO output tracks the input frequency. Any frequency changes at the input are immediately detected and the VCO frequency is adjusted to reduce the error to zero.

The two ranges of frequency used in the PLL are the "lock range" and the "capture range." The lock range is the range of frequencies that the VCO can generate. Once lock has occurred, the VCO will remain locked to any incoming frequency within the "lock range." The capture range is smaller than the lock range and represents the range of frequencies that the VCO can track before lock has occurred.

In this experiment we will study the characteristics of the phase-locked loop and the effect changes in the input frequency have on the DC output signal.

Lab Procedures

NOTE: The schematic, block diagram, protoboard layout, lab questions, and table are at end of this document. The circuit will be constructed on a protoboard module that uses wire jumpers to make connections between contacts. Strip both ends of the required jumper and connect to the indicated points. Keep wires neat and short to improve circuit operation and aid in troubleshooting when required.

FREE-RUNNING FREQUENCY MODE

1. Construct the circuit shown at the end of this procedure using two 0.1 μF capacitors in parallel for C_F.

2. Use the formula $f = \frac{0.3}{R_T C_T}$ to calculate the free-running frequency of the PLL when R_T is equal to 1 kΩ and the potentiometer is at its extremes. C_T is the capacitor from Pin 9 to ground.

3. Record the data in Table 1.

4. With the function generator disconnected, the 565 will be in the free-running operational mode. Connect the oscilloscope to pin 4.

5. Measure the output frequency with the potentiometer at both of its extremes.

6. Record the frequencies in Table 1.

7. Vary the potentiometer and observe the changes in the frequency at Pin 4.

8. Adjust the potentiometer to obtain a 5 kHz signal at Pin 4.

LOCK RANGE

9. Connect the function generator.
10. Observe the signal on Pin 2.
11. Adjust the output of the function generator to a 0.5 V_{P-P} at 5 kHz.
12. Observe the output signal on Pin 4.
13. Vary the output signal of the function generator from 4 kHz to 6 kHz. Notice how the PLL output is locked onto the free-running frequency.
14. The loss of lock will produce a "jittery" waveform on the oscilloscope. Lock will be gained (at the low frequency) when the jitter stops and lost (at the high frequency) when the jitter begins.
15. Measure these maximum and minimum LOCK frequencies.
16. Record the measured values in Table 2.

CAPTURE RANGE

17. The internal 3.6 kΩ resistance and the value of C_F determine the cutoff frequency of the low pass filter. This filter removes the original frequencies, their harmonics, and the sum frequency. Use the equation: $f = \frac{1}{2\Pi 3.6kC_F}$ to determine the cutoff frequencies of the filter with the following C_F capacitor values: 2 μF, 0.1 μF, and 0.047 μF. Remember that two 0.1 μF capacitors connected in parallel are equal to 0.2 μF.

18. Record the calculated values in Table 3.

Table 1: Free-Running Mode

Equation: $f = \frac{0.3}{R_T C_T}$

Potentiometer Wiper	Calculated f	Measured f
UP		
DOWN		

Table 2: Lock Range

f_{MAX}	
f_{MIN}	

Table 3: Capture Range

Equation: $f = \frac{1}{2\Pi 3.6 k C_F}$

C_F	f_C	f_{MAX}	f_{MIN}
0.2 µF			
0.1 µF			
0.047 µF			

Post Lab Questions

1. The maximum calculated "lock" frequency is
   a. 3.10 kHZ
   b. 6.38 kHz
   c. 6.66 kHz
   d. 7.12 kHz

2. How does the "capture range" compare to the "lock range"?
   a. Smaller
   b. Same
   c. Larger
   d. None of these

3. If the cutoff frequency of the low-pass filter increases, the capture range
   a. Decreases
   b. Stays the same
   c. Increases
   d. None of these

4. The capacitor that controls the free-running state frequency of the VCO is
   a. C_F
   b. C_T
   c. Input coupling capacitor
   d. Bypass capacitor

CONCLUSION: Write a short paragraph comparing your observations to the calculations using percentage of variation and waveforms to explain your conclusion.

PLL Circuit Schematic