Enhancement Mode MOSFET Transistors

Acknowledgements: Developed by Ronnie Wilson, Faculty of Austin Community College, Austin, Texas.

Lab Summary: The purpose of the laboratory experiment is to introduce the concepts associated with the Enhancement Mode Metal Oxide Semiconductor Field Effect Transistors. Calculations will be made to determine some of the parameters associated with the E-MOSFET being tested. In addition, circuits using E-MOSFET transistors are tested to determine the operating characteristics of the transistor.

Optional Written Report: At the completion of the laboratory experiment, the student may be asked to develop a written report of findings associated with the circuits tested and the determination of the electrical characteristics associated with an E-MOSFET transistor

Lab Goal: The goal of this lab is to observe the operation of E-MOSFET transistors and to perform measurements of the parameters associated with the operation of the transistors and the associated circuits.

Learning Objectives

1. Measure the input resistance of an E-MOSFET transistor.
2. Measure the ON resistance of an E-MOSFET transistor.
3. Measure the values of I_D and V_{DS} required to calculate the value of *k* for the transistor.
4. Test the electrical parameters associated with an amplifier.
5. Test the electrical parameters associated with digital circuits that utilize an E-MOSFET transistor.

Grading Criteria: Your lab grade will be determined by your performance on the experiment, the lab questions, and the content and quality of your laboratory report (if assigned).

Time Required: 3 to 4 hours

Special Safety Requirements

Static electricity can damage the MOSFET devices used in this lab. Use appropriate ESD methods to protect the devices.

No serious hazards are involved in this laboratory experiment, but be careful to connect the components with the proper polarity to avoid damage.

Lab Preparation

- Read the WRE MOSFET Module.
- Read this document completely before you start on this experiment.
- Acquire required test equipment and appropriate test leads.

- Gather all circuit components and the breadboard or electronic trainer.
- Review the ESD material in the Metal Oxide Semiconductor Field Effect Transistors module related to the proper handling of MOSFETs.
- Print out the laboratory experiment procedure that follows.

Equipment and Materials

Note for Instructor: Each group of students will need the parts listed below.

Part	Quantity
Digital Multimeter (DC Voltage)	1
Variable DC Power Supply (Minimum 15 Volt)	3
Oscilloscope (20 MHz)	1
Electronic Trainer or Breadboard	1
Hookup Wire	As required
CD4007 CMOS Integrated Circuit	1
Fixed Resistor 1 kΩ	1
Fixed Resistor 10 kΩ	1
Variable Resistor 10 kΩ (Multiturn preferred for improved control)	1
LM741 Op-AMP	1

Introduction

E-MOSFET devices operate on the principle that a conduction path between the drain (D) and source (S) does not exist until an adequate voltage equal to V_{th} is applied between the gate (G) and the source.

As the value of V_{GS} is increased, the conduction channel between the drain and source will increase allowing more current to flow from drain to source.

The circuit used in this lab will illustrate the relationship of V_{th} and R_{ON} for different applications of an E-MOSFET.

Lab Procedure

Note: All tables, lab questions, and schematic drawings are shown at the end of this procedure.

1. Access the Texas Instrument web site at www.ti.com. Locate the data sheet for a CD4007UB CMOS Integrated Circuit.
2. Install a CD4007 CMOS integrated circuit onto the breadboard with its leads connected to a separate row of the board.
   a. Use the data sheet for the CD4007UB integrated circuit to determine the pin out for one of the N-channel MOSFETs.
   b. Apply the red lead of the high impedance digital multimeter meter to the gate

c. Measure the resistance between the gate and source terminals. Enter the values in row one of Table 1.

d. With the red lead still on the gate, measure the resistance between the gate and drain terminals. Enter the values in row 1 of Table 1.

e. Apply the red lead to the drain and measure the resistance between the drain and source terminals. Enter the values in row 1 of Table 1.

f. Apply the black lead of the digital multimeter meter to the gate

g. Measure the resistance between the gate and source terminals. Enter the values in row two of Table 1.

h. With the black lead still on the gate, measure the resistance between the gate and drain terminals. Enter the values in row 2 of Table 1.

i. Apply the black lead to the drain and measure the resistance between the drain and source terminals. Enter the values in row two of Table 1.

j. Review the resistance reading entered in Table 1. Answer questions 1, 2, and 3 at the end of this procedure.

3. Use the data sheet for the CD4007 to determine the type of MOSFET transistors that are used in this chip.

a. Enter the type of MOSFET transistors used in the chip: _____

b. In order to verify the type of transistor inside the chip, perform an electrical test on the transistor. This will provide information about the relationship between V_{GS} and I_D.

c. To determine this relationship, use the circuit in Figure 1 and the following procedure to test both the P and N-channel MOSFET transistors.

d. Determine the threshold voltage, $V_{th,}$ for the transistors in the CD4007 chip using Figure 2.

i) Begin the test by turning the power supply voltage to zero and measure the voltage across the 1 kΩ resistor and the voltage V_{GS}. Enter the value in Table 2 at the end of this procedure.

ii) Increase the power supply voltage, V_{DD} until the voltage across the resistor **just** begins to increase. Measure the voltage across the resistor and V_{GS} and enter the value in Table 2.

iii) Continue to increase V_{DD} in small increments and record your results in Table 2.

iv) When the voltage across the resistor increases linearly with the increase in V_{DD}, continue to take readings until V_{DD} reaches 18 Volts.

v) Graph your results in Graph 1 with V_{GS} on the horizontal axis and I_D on the vertical axis. Use the results of your graph to answer questions 4 and 5.

e. Construct the circuit shown in Figure 3.

i) Begin the test by turning the power supply voltage to zero and measure the voltage across the 1 kΩ resistor and the voltage V_{GS}. Enter the value in Table 3 below.

ii) Increase the power supply voltage, V_{DD} until the voltage across the resistor **just** begins to increase. Measure the voltage across the resistor and V_{GS} and enter the value in Table 3.

iii) Continue to increase V_{DD} in small increments and record your results in Table 3.

iv) When the voltage across the resistor increases linearly with the increase in V_{DD}, continue to take readings until V_{DD} reaches 18 Volts.

v) Graph your results in Graph 2 with V_{GS} on the horizontal axis and I_D on the vertical axis. Use the results of your graph to answer questions 6 and 7.

MOSFET Logic Gates

To understand a MOSFET transistor operation as a switch in a logic circuit, you will use the circuit shown in Figure 4. In this section of the lab, you will measure the output voltage of an inverter constructed from MOSFET transistors. During the measurement of the voltages associated with this circuit, you are interested in the threshold voltages where the transistors switch and V_{out} vs. V_{in} is equal to -1.

The 741 op-amp is configured as a voltage follower; therefore, its output should remain relatively constant as I_D varies.

Lab Procedure

1. Construct the circuit shown in Figure 3 at the end of this procedure.
2. Measure the voltages V_{in} and V_{out} over the range of V_{in} from 0 to V_{DD}. By measuring the voltage across R_2 you can calculate the value of I_D for the circuit since $I_D = I_{R2} – I_{R1}$ and $I_{R1} = V_S/R_1$.
3. Set V_S = to a value of 12 V. As you perform the lab, monitor V_S to be sure it remains constant while making measurements.
4. Enter the values in Table 4.
5. Plot the values of V_{in} vs. V_{out} for the data in Table 4 in Graph 3. Answer question 8.

The E-MOSFET can be used to implement a NOR gate as shown in Figure 4. The operation of the circuit follows the digital logic for a standard NOR gate.

6. Build the circuit shown in Figure 4.
   a. Set V_{DD} = 5 V and let binary 1 = 5 V and binary 0 = 0 V.
   b. Apply all possible combination of inputs to the circuit and determine if the output is correct.
   c. Apply a square wave to input A at a low frequency of approximately 100 Hz.
   d. Increase the frequency until you experience the Miller effect. Answer question 11.
7. Answer the Post Lab Questions.
8. Do the Optional Report if it is assigned by your instructor.

Table 1: MOSFET Resistance

Meter Polarity	Gate - Source	Gate - Drain	Drain - Source
Forward			
Reverse			

Table 2: MOSFET Basic Parameters: N-Channel

V_{DD}	V_{DS}	$V_{RESISTOR}$	I_D	V_{DD}	V_{DS}	$V_{RESISTOR}$	I_D

Table 3: MOSFET Basic Parameters: P-Channel

V_{DD}	V_{DS}	$V_{RESISTOR}$	I_D	V_{DD}	V_{DS}	$V_{RESISTOR}$	I_D

Table 4: MOSFET Inverter Circuit

V_{in}	V_{out}	V_{R2}	I_{R2}	I_{R1}	$I_D = I_{R2}-I_{R1}$	V_{in}	V_{out}	V_{R2}	I_{R2}	I_{R1}	$I_D = I_{R2}-I_{R1}$

Table 5: MOSFET NOR Gate Circuit

V_A	V_B	V_{out}

Lab Questions

1. Do these reading indicate you have a diode protecting the input of the CD4007?

2. Do the resistance readings in table 1 indicate the transistors inside of the CD4007 are a D-MOSFET or an E-MOSFET?

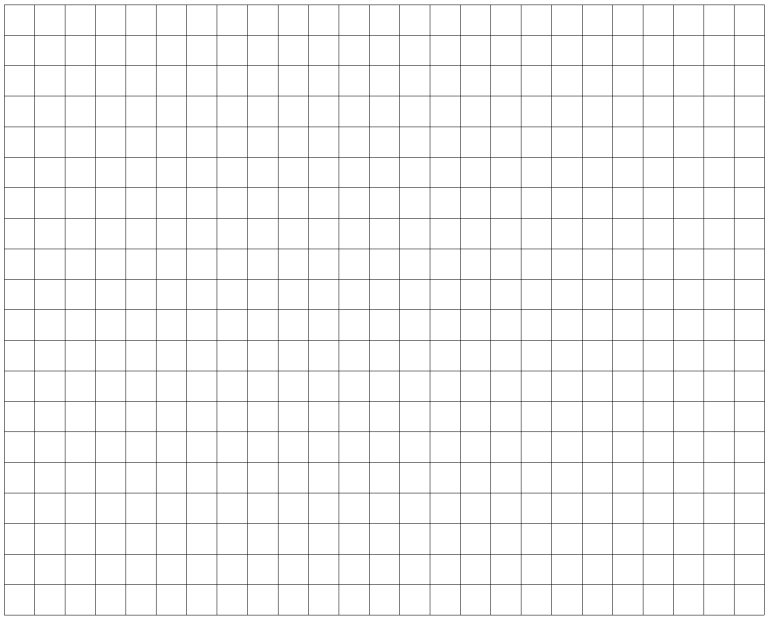
3. Explain how these measurements indicate the type of transistor present.

Graph 1: V_{GS} on the horizontal axis and I_D on the vertical axis

4. Determine the value of the threshold voltage and enter the results. V_{th} = _____

5. From the data obtained from circuit 1, calculate the ON resistance for the transistor under test.
   R_{ON} = _____

Graph 2: V_{GS} on the horizontal axis and I_D on the vertical axis



6. Determine the value of the threshold voltage and enter the results. V_{th} = _____

7. From the data obtained from circuit 2, calculate the ON resistance for the transistor under test.
R_{ON} = _____

Note: The drain current for an E-MOSFET is related to V_{GS} by the following equation:

$$I_D = k\left(V_{GS} - V_{th}\right)^2$$

The value of *k* can be determined from the graph of V_{DS} vs. $\sqrt{I_D}$. The linear section of the slope of the curve represents the value of $\sqrt{k}$.

Graph 3: V_{in} vs. V_{out}

8. What does this graph represent and what does it demonstrate about the inverter circuit?

9. Using circuit 5, determine when the circuit will consume the maximum current.

10. Predict how the circuit will operate if you applied a square wave to input A while holding input B at a binary 1.

11. Explain what happened to the circuit when you increased the frequency until you experienced the Miller effect.

Post Lab Questions

1. Review the results you obtained when determining the MOSFET resistance. What do these reading indicate about a MOSFET compared to a bipolar transistor?

2. Why was a voltage of V_{th} required to cause current to flow from Drain to Source when you measured the value of V_{th} for both the P- and N-channel transistors?

3. As you tested the circuit in Figure 3 you found the voltage out of the op-amp would drop and then return to its original value when V_{in} was at its minimum and maximum values. Why?

Optional Written Report

Write a report, which describes how you would use the knowledge you have gained in the WRE Metal Oxide Semiconductor Field Effect Transistors module experiment. Your report should include discussions which relate the threshold voltages and the R_{ON} for both types of transistors.

Relate the data obtained in this experiment to the performance of the inverter's noise margins. Information relating to the V_{th} value and the inverter circuit noise margin used in this experiment can be found on the internet.

Discuss in your report the affect Miller's effect had on your NOR gate circuit as you increased the input frequency of the input signal.

Schematic Figure 1:

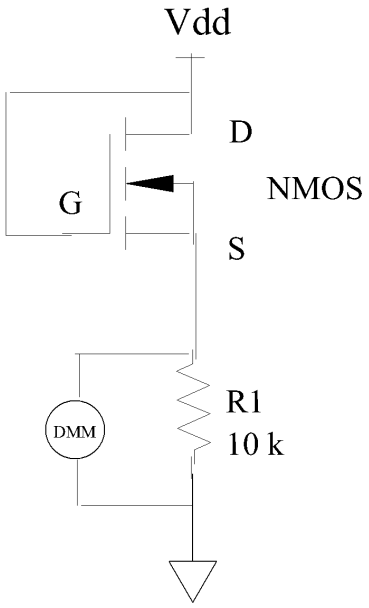


Figure 1

Schematic Figure 2:

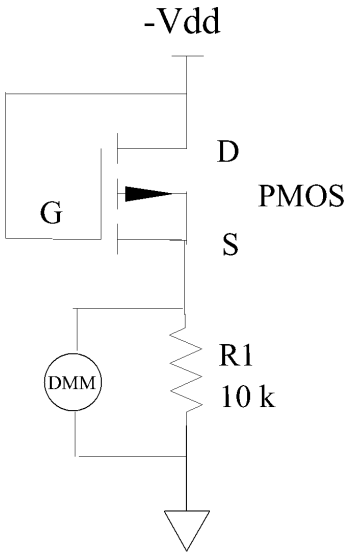


Figure 2

Schematic Figure 3:

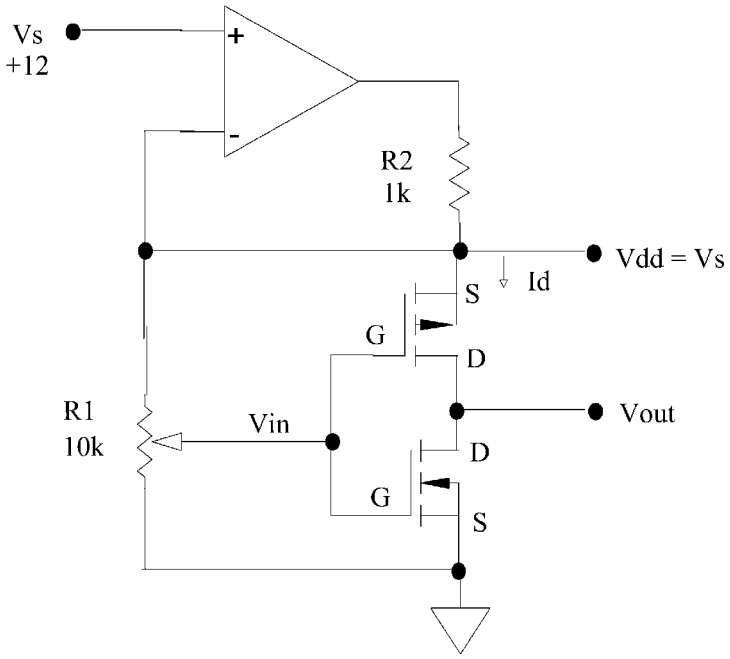


Figure 3

Schematic Figure 4:

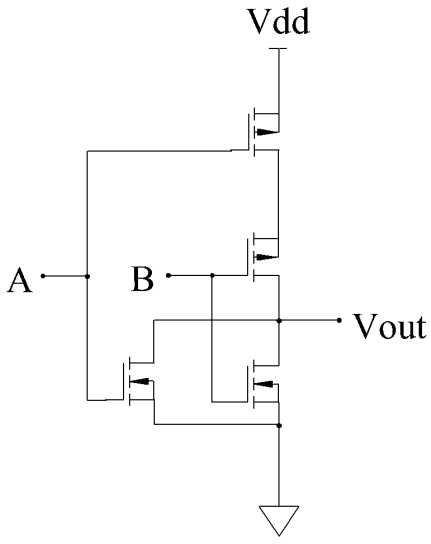


Figure 4