# Phase-Locked Loop Applications

# Applications of PLLs

Virtually every piece of electronic equipment in use today contains one or more PLLs. PLLs are used in personal computers, radios, TV sets, video monitors, cable and satellite TV boxes, cell phones, VCRs, CD, DVD and MP3 players.

Depending on the application, the PLL can be used as a band pass filter, clock and data recovery circuit, FM demodulator, clock multiplier, or a frequency synthesizer.

# PLL as a Band Pass Filter

Because of the capture range characteristic of the PLL, it is an excellent band pass filter (BPF). It allows signals within the capture range to pass through while effectively eliminating those signals whose frequencies are above and below the capture range.

When used as a BPF, the PLL does not simply process the existing signal into an output as an RC or LC filter does. Instead, the PLL produces an entirely new and different signal (the VCO output) that has exactly the same frequency as the input.

# PLL as a Band Pass Filter

The PLL is widely used in electronics to clean up and rejuvenate signals that have been attenuated, distorted, and otherwise compromised during transmission or processing. The PLL is very effective at eliminating noise and interference from signals.

The bandwidth of the circuit is set by the capture range and the loop filter characteristics.

Most applications of the PLL as a BPF occur in the communications field where analog signals are processed or transmitted.

# Clock and Data Recovery (CDR)

The filtering characteristics of a PLL are also used with digital signals. Specifically, the PLL is often used to recover and rejuvenate the clock signal in a digital system or data communications system

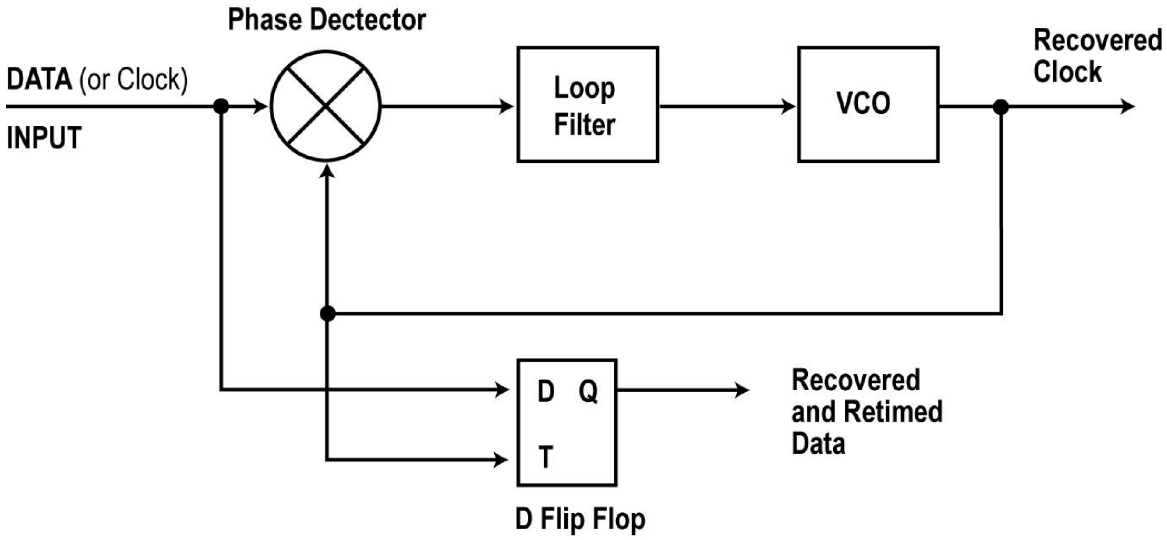
The clock signal is a stable rectangular wave at a precise frequency as set by a quartz crystal. It is used as the main timing signal in any computer or digital system.

# Clock and Data Recovery (CDR)

Clock signals deteriorate as they are transmitted over long distances, either over long traces on a printed circuit board (PCB), between several PCBs, or over long cables. To be effective in timing, these signals must be clean, noise and jitter free, and have sharp rise and fall times.

In data communications systems like the Internet, the clock signal is usually inherent in the data transmitted. That is, the clock must be extracted from the data signal at the receiver.

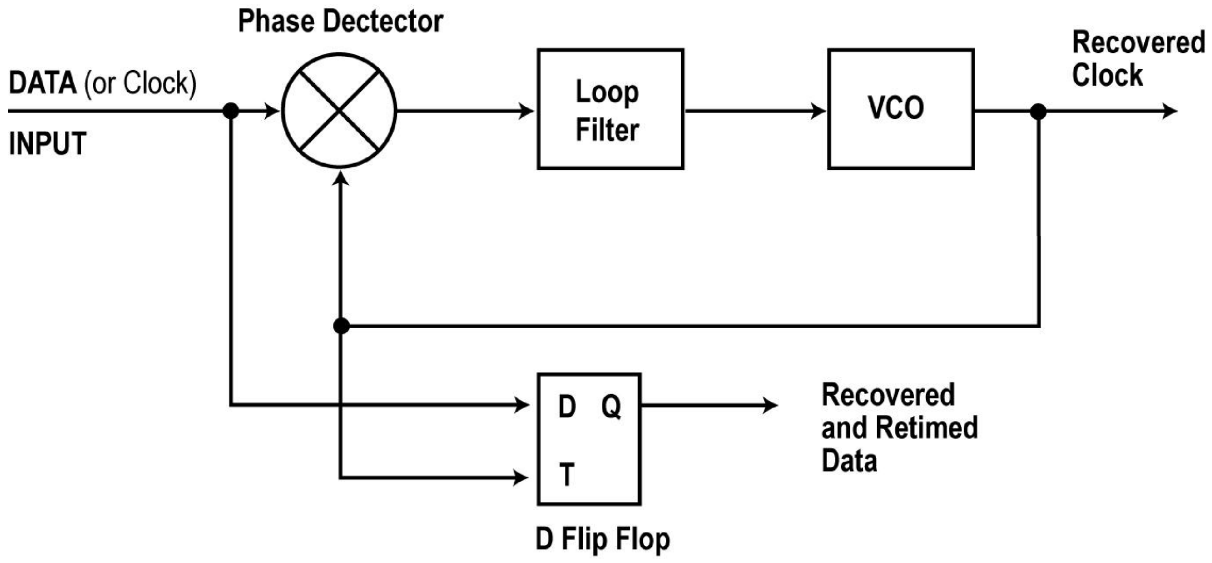
# PLL CDR




By putting the compromised clock signal into a PLL, the filtering action cleans the signal. The VCO develops a new clean, fast, rectangular clock signal. Any data input can be also be rejuvenated and retimed.

It is used to recover the clock from the data signal. The recovered clock is used to retime the received data.

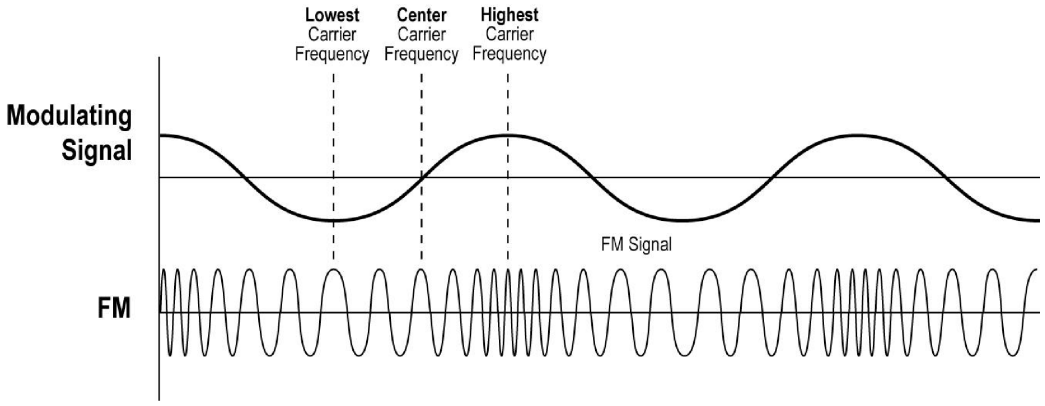
# PLL CDR




The VCO output is the rejuvenated clock. A D-type flip flop triggered by the clock is used to recover and retime the data.

While CDR circuits are available in individual IC format, most are actually built into other larger systems ICs.

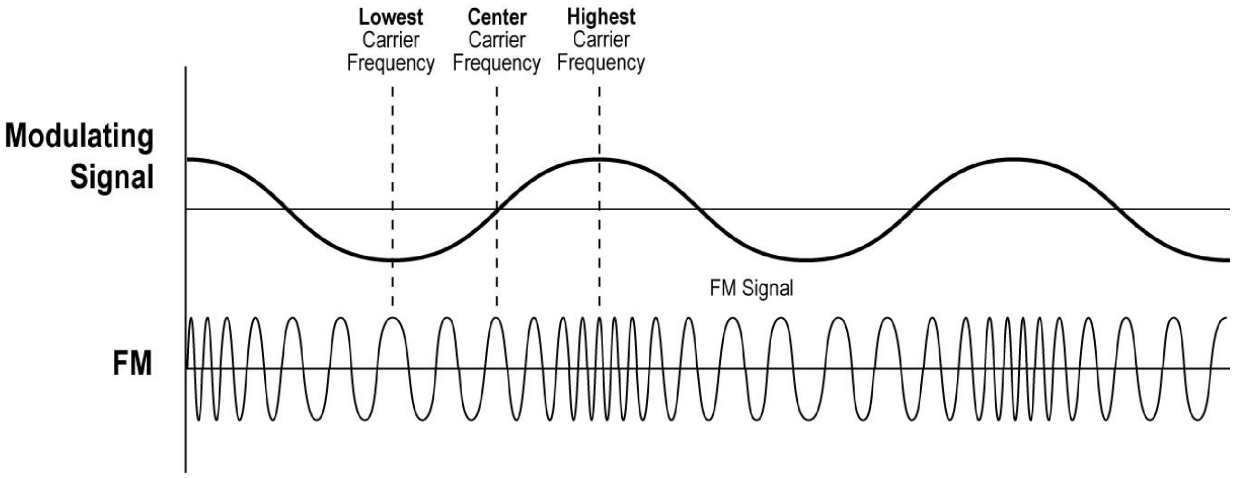
# FM Demodulator




Frequency modulation (FM) is one of the more widely used types of modulation in electronics. It is used in FM broadcast radio and TV, mobile radios, communications receivers, some data communications applications, and some tape recording systems (VCRs).

In FM, the transmitted signal is used to vary the frequency of an oscillator operating at a much higher frequency. The higher frequency is called the carrier.

# FM Demodulator

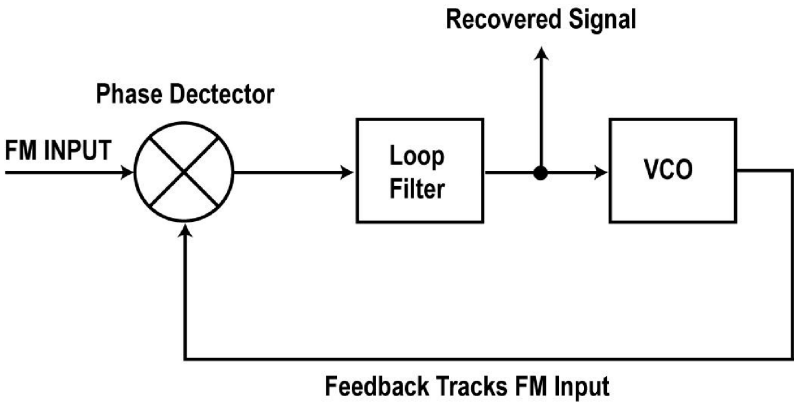



The carrier frequency is varied above and below the center frequency. The variation is proportional to the amplitude of the modulating voice, video, or data signal.

The FM signal is transmitted to the receiver by radio or by cable.

At the receiver, the signal is amplified, filtered, and processed. A demodulator circuit is needed to recover the original modulating signal.

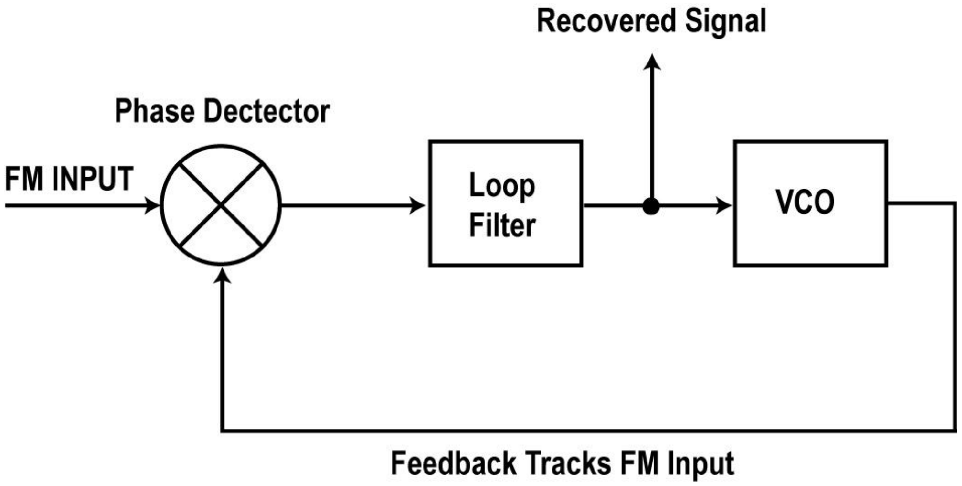
# FM Demodulator




A wide variety of FM demodulator circuits have been developed over the years to detect and recover modulating signals from an FM carrier. Most of those older original circuits are no longer used and have been replaced by the PLL.

The PLL is used in its normal configuration where the FM signal is applied to the phase detector input. As the carrier frequency varies, the VCO output tracks it exactly.

# FM Demodulator




As the VCO follows the FM signal, the loop filter output varies in exactly the same way as the original modulating signal. In other words, the VCO is serving as a carrier oscillator that is being modulated by the original signal.

The output of the loop filter therefore is the recovered modulating voice signal.

A key benefit of the PLL in this application is that the circuit is essentially noise free because it also serves as a band pass filter.

# Clock Multiplier

The PLL can also be used as an effective frequency multiplier.

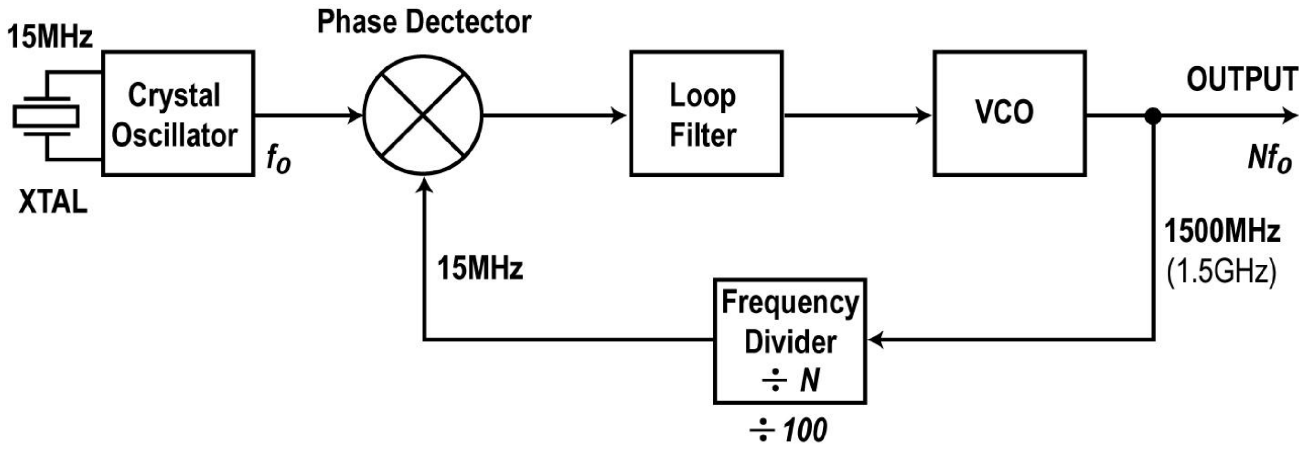
A frequency multiplier is a circuit that multiplies some input frequency by some fixed integer value.

Frequency multipliers are used in applications where physical limitations of components or circuits restrict or prevent operation at higher frequencies.

A common application of the PLL is to multiply the frequency of a clock signal in a computer or data communications system. In this application, the PLL is called a clock multiplier.

Crystal oscillators are used to obtain a highly stable and precise operating clock. However, the frequency range of a quartz crystal is limited by its physical thickness. The typical upper frequency range is about 150 MHz.

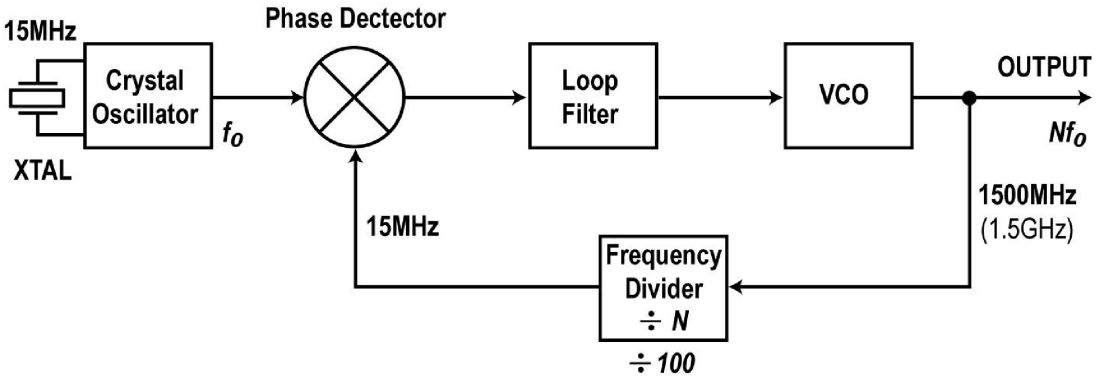
# PLL as a Clock Multiplier




When a PLL is used as a clock multiplier, the input is from a stable crystal oscillator (XTAL).

The VCO output is not connected directly to the phase detector input as in a standard PLL. Instead, the VCO output is connected to a digital frequency divider. The divider output is connected to the second phase detector input.

# PLL as a Clock Multiplier

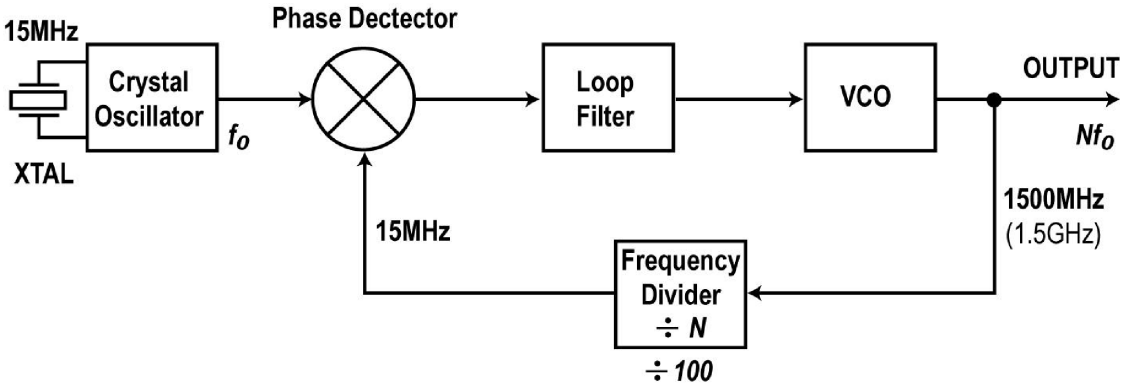



The divider is usually a counter or shift register made with flip flops. It may also be made with logic circuits, exist as a separate IC, or be fully integrated into a larger IC chip.

The divider takes the input signal and reduces its frequency by some integer division factor N such as 100.

Since the phase detector inputs must be at the same frequency for proper operation and lock, the divider input must be higher in frequency by a factor of N.

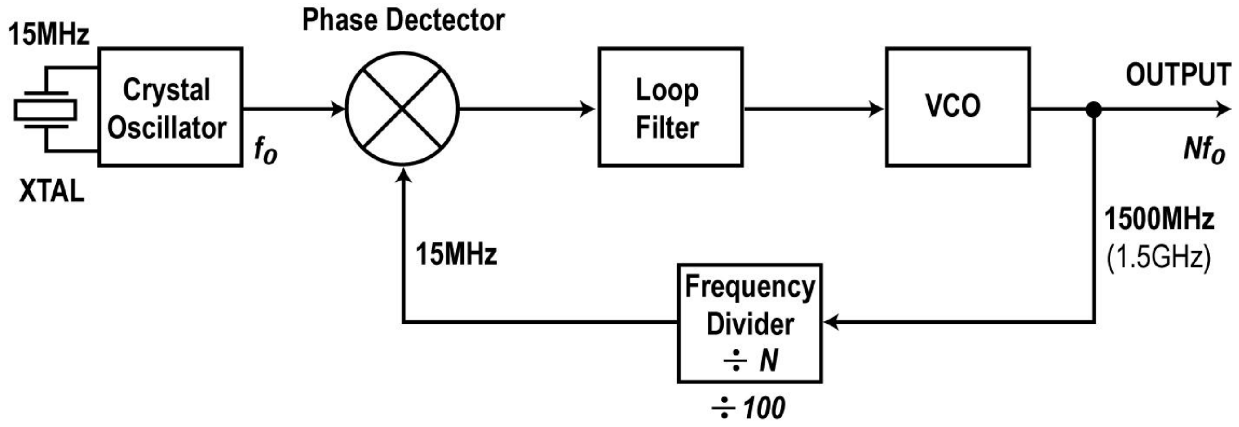
# Example: PLL as a Clock Multiplier




In this example, a 15 MHz crystal oscillator is applied to the input and the divide ratio is 100. Therefore the VCO output must be 15 x 100 = 1500 MHz or 1.5 GHz. This output is divided by 100 to produce the 15 MHz signal for the phase detector.

Clock multipliers are widely used to obtain very high frequency clock signals beyond the capability of a standard crystal oscillator. Because the PLL tracks the input, the VCO output has the same precision and stability as the input crystal frequency.

# PLL as a Clock Multiplier




A clock multiplier is used in PCs to obtain the clock. For example, a 1.5 GHz Pentium processor needs a stable 1.5 GHz clock. Usually the PLL multiplier is integrated with the crystal and oscillator.

Clock multipliers are also widely used in fiber optic data communications systems with clock rates up to 10 GHz.

# Frequency Synthesizers

A frequency synthesizer is a circuit that generates a sine or rectangular wave output whose frequency can be easily varied in steps by an external input.

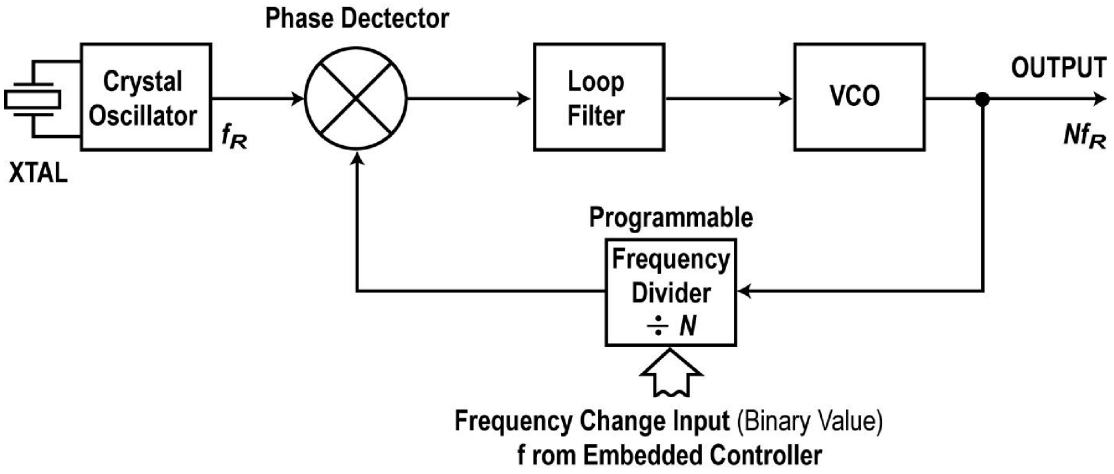
A frequency synthesizer is similar to an oscillator but its frequency cannot be varied continuously. Instead, the frequency is varied in predetermined increments.

Frequency synthesizers have the stability and precision of a single frequency crystal oscillator.

The most common application of a frequency synthesizer is to vary the operating frequency of the receiver or transmitter in a communications application.

Every radio, TV, or cell phone uses a frequency synthesizer to set its frequency of operation.

# PLL as a Frequency Synthesizer

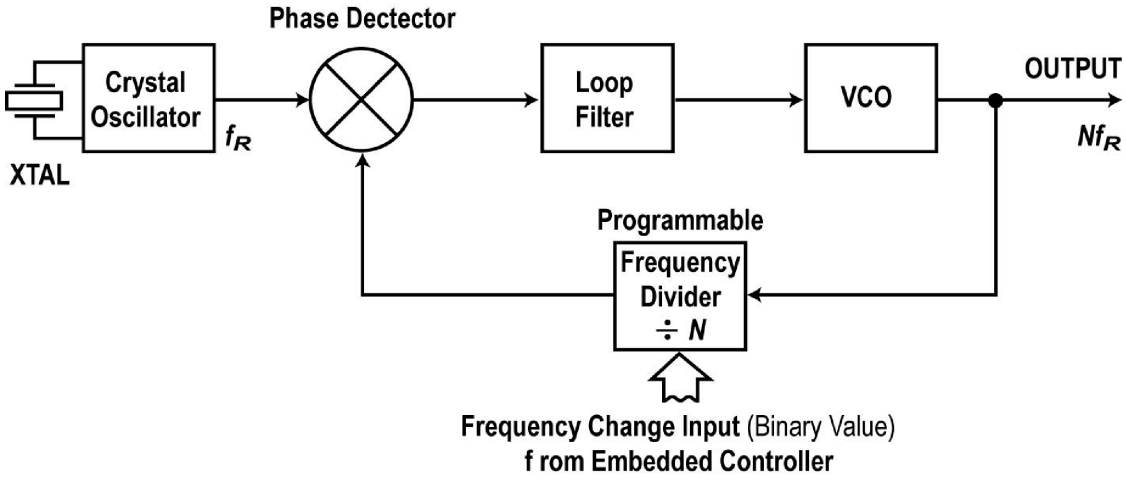



The configuration of a PLL as a frequency synthesizer is similar to the configuration used in a multiplier.

The input to the PLL is a crystal oscillator used as a reference to establish the precision and stability of the output.

The crystal input frequency $f_R$ also establishes the step or increment of output frequency change.

# PLL as a Frequency Synthesizer




The frequency divider in the feedback path between VCO output and phase detector input is programmable. The divide ratio N can be changed by a binary input value. Changing the frequency division factor changes the output frequency.

The output frequency $f_o$ is equal to the divide ratio multiplied by the reference frequency or $f_o = N \times f_R$.

# Example: PLL as a Frequency Synthesizer

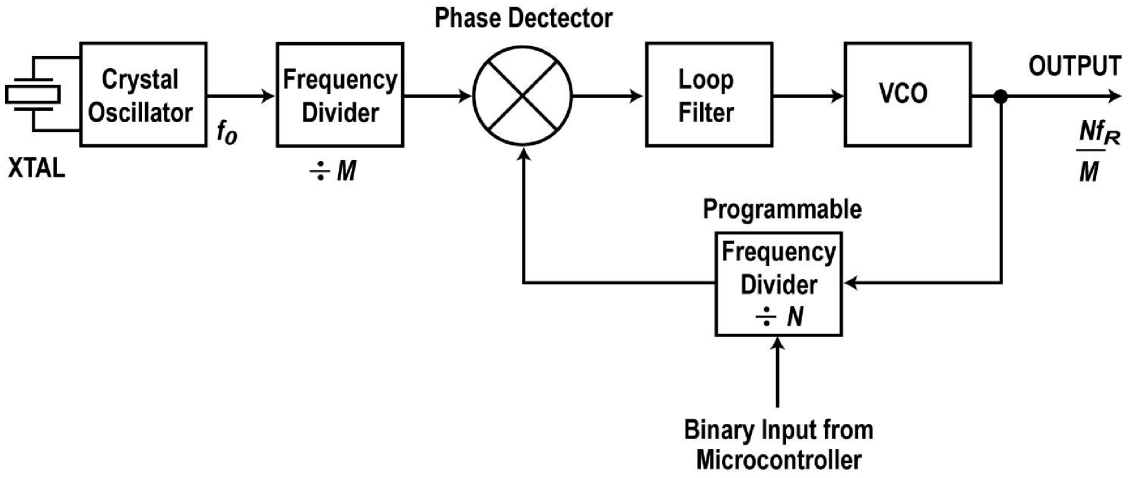
With a 1 MHz reference crystal oscillator and a divide ratio of 1024, the output frequency is 1 MHz x 1024 = 1024 MHz or 1.024 GHz.

Changing the divide ratio N changes the output frequency in 1 MHz increments. Changing N to 1023 causes the new output to be 1023 MHz or 1.023 GHz.

Even though the divide ratio can be changed by a manual switch, it is usually changed by giving the divider circuit an appropriate binary input number. That number may be loaded either in parallel or serially from an embedded microcontroller.

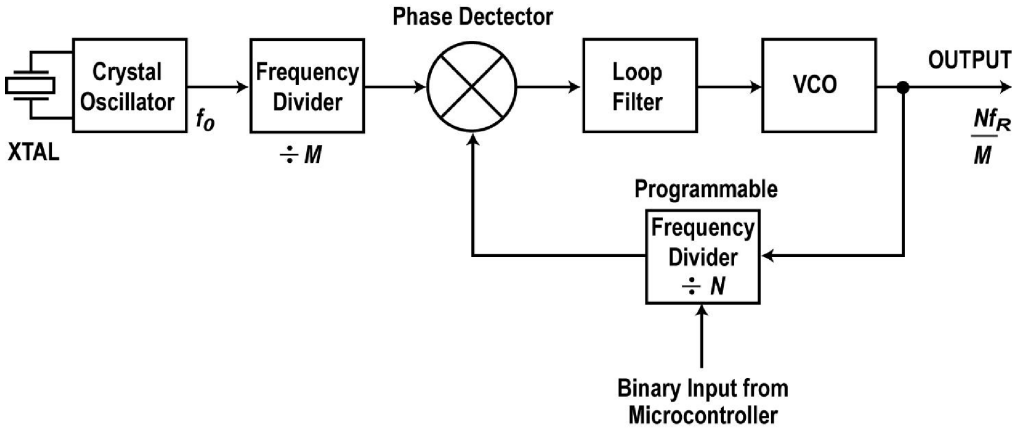
The output frequency increment of change is equal to the reference input to the phase detector.

# PLL Synthesizer




In some systems, a smaller incremental step is desired. Since quartz crystals are not available below about 100 kHz, a higher frequency crystal is used and a fixed frequency divider with a divide ratio of M is added between the crystal oscillator and the phase detector input. The synthesizer output is $f_o = (N/M)f_R$

# Example: PLL Synthesizer

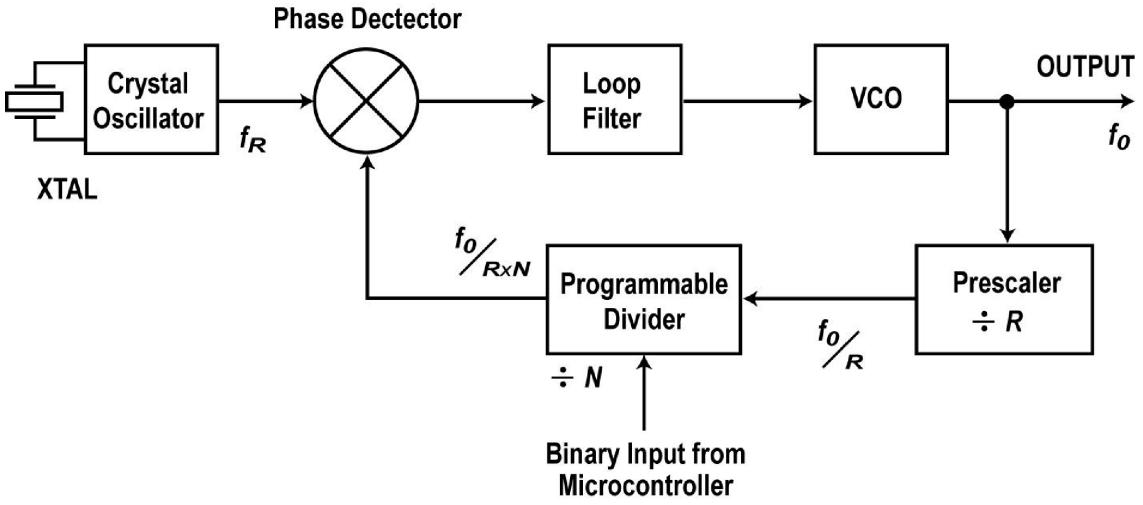



With a 3 MHz crystal, an input divide ratio M or 100 and a divide ratio N of 400, the output is (400/100)3 MHz = 12 MHz.

With this arrangement, the actual reference frequency is 3 MHz/100 = 30 kHz. The output will change in 30 kHz increments as N is changed.

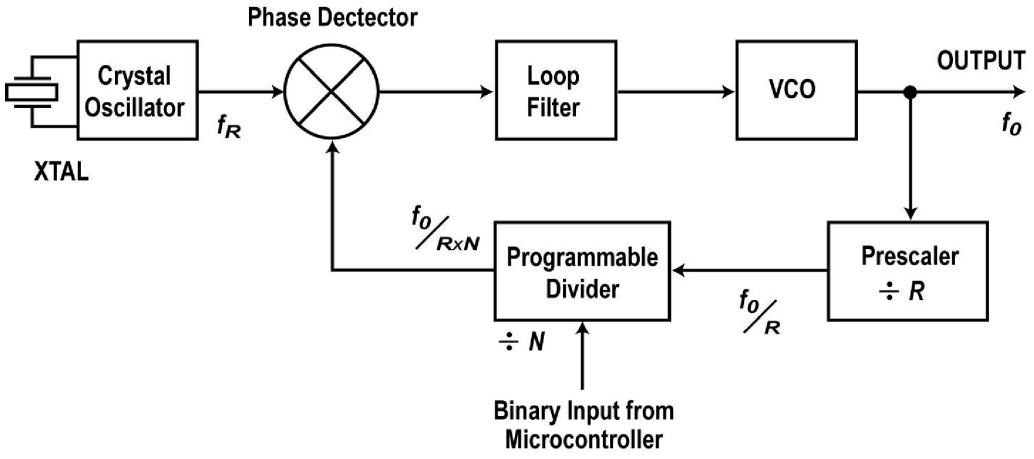
With N set to 401, the output frequency will be 12.03 MHz. If N = 402 the output is 12.06 MHz.

# PLL with Prescaler



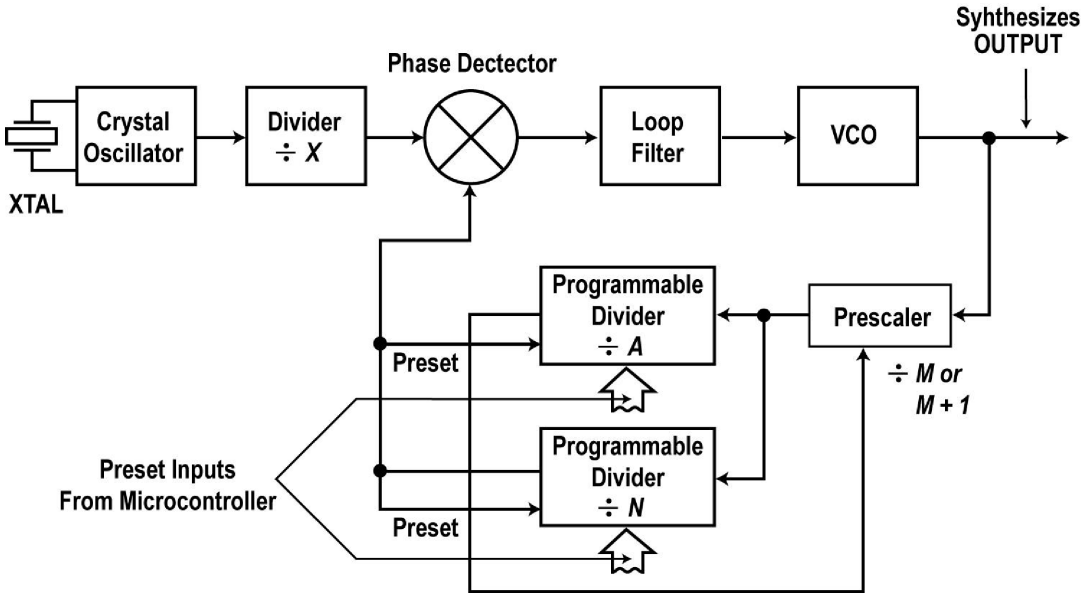

In some designs where the output frequency is very high, a fixed ratio divider is connected between the VCO output and the input to the programmable divider. This divider is called a prescaler. It reduces the output frequency (by a factor of R) to a level that can be handled by the programmable divider.

# PLL with Prescaler




The output frequency then is $f_o = f_R$ x N x R. Since R is fixed, changing N results in a frequency output increment step that is $f_R$ x R. This can be corrected for by adding a divider equal to R between the reference input and the phase detector. This lowers the comparison frequency in the phase detector and that, in turn, slows the loop response to a division ratio change.

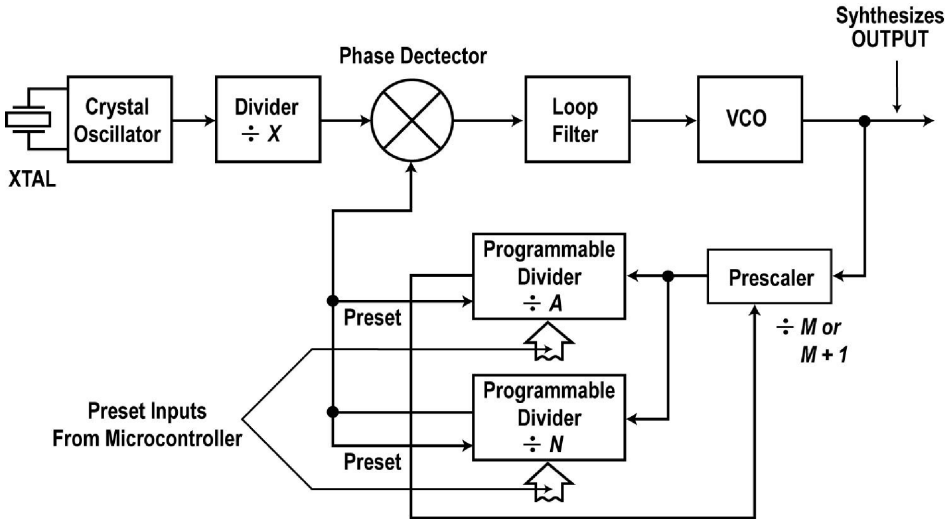
# Fractional-N PLL




A variation of the PLL synthesizer that keeps the output increment step equal to the phase detector input is the fractional-N divider.

The fractional-N PLL uses a prescaler that can be set to a value of M or M+1. The output of this divider goes to a programmable divider that can be set to divide by A. The output of this divider is used to control the divide ratio of the prescaler.

# Fractional-N PLL




A second programmable divider is connected to the output of the prescaler. It can be set to any divide ratio N.

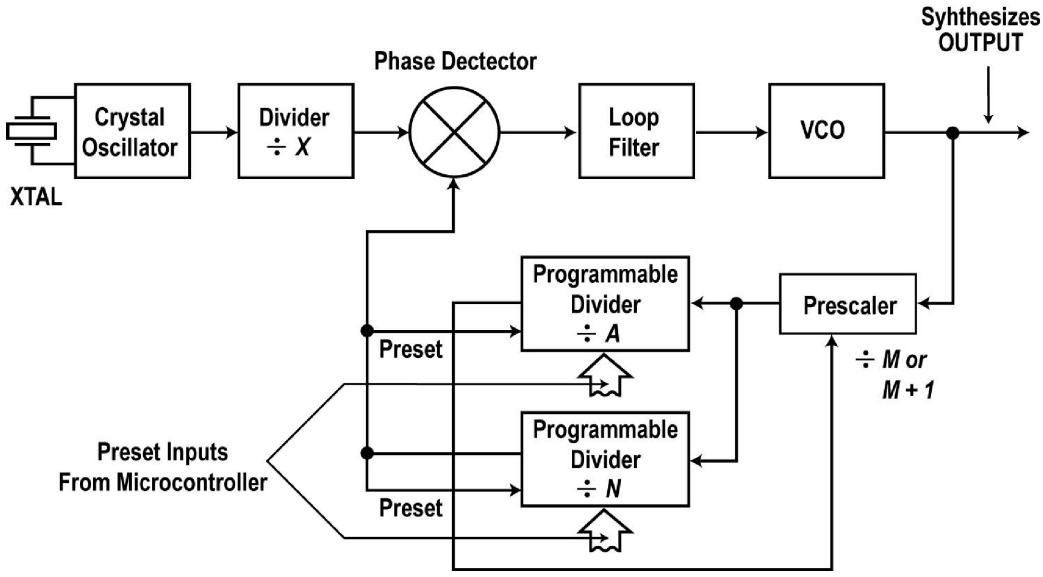
Both the A and N dividers are down counters that are loaded with an initial count and are then decremented to zero where they recycle.

The divide ratio A is always less than the divide ratio N.

The overall divide ratio between the VCO output and the phase detector input is R = NM + A.

The output frequency is $f_o = f_R \times R$.

# Fractional-N PLL Operation

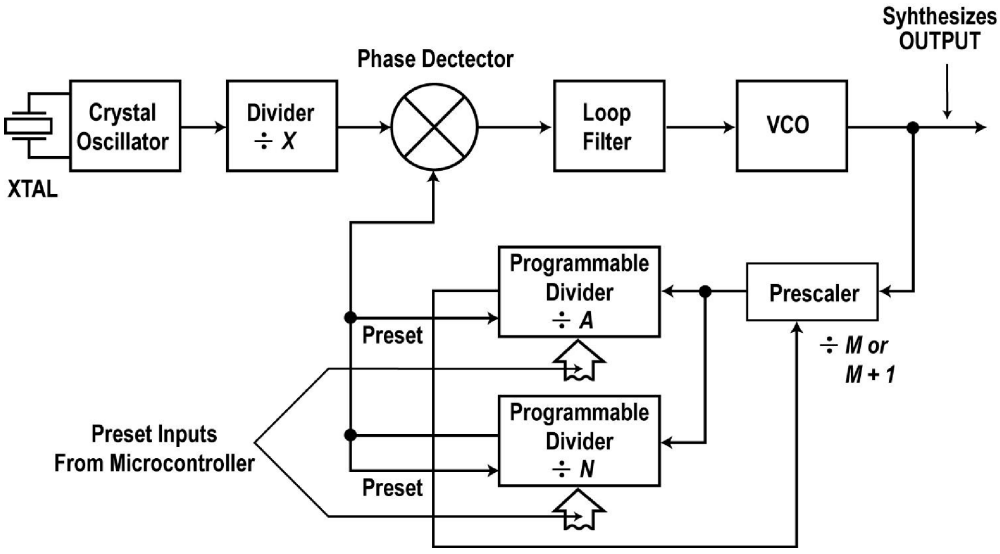



Assume M = 64 and M+1 = 65, A =10 and N = 200. The reference frequency is 13 MHz.

The A and N dividers are loaded from an external source such as a microcontroller.

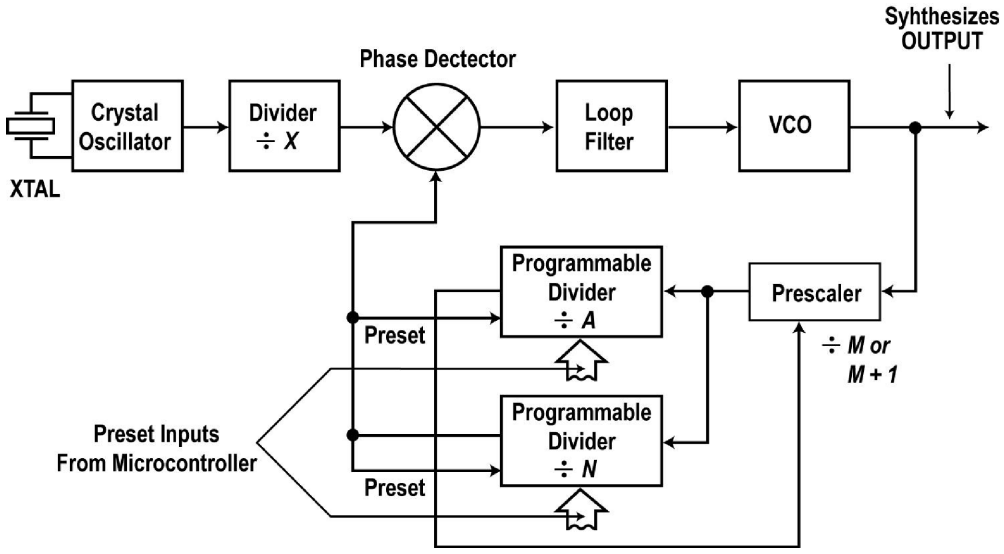
The prescaler is initially set to M+1 or 65.

# Fractional-N PLL Operation




The output from the VCO is initially divided by 65 (M+1). The prescaler output is fed to both the A and N dividers. Since A (10) is less than N (200), the A divider is decremented to zero first. When zero occurs, the A divider output changes the prescaler ratio to M (64). The down counting continues until N is decremented to zero at which point the sequence is repeated.

# Fractional-N PLL Operation

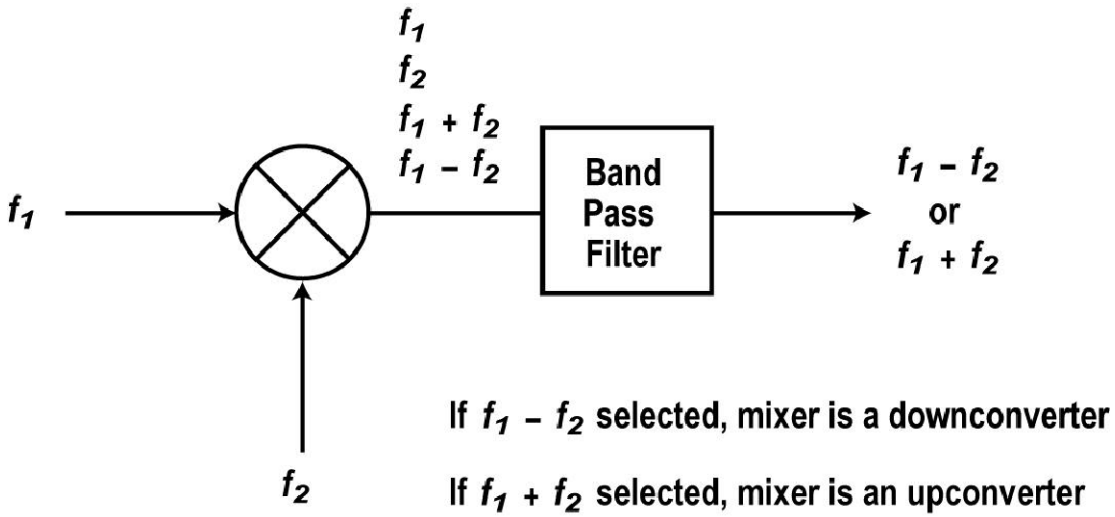



The N divider output is used to preset the A and N values into the programmable down counters at the end of a cycle.

When M = 64, A =10, and N = 200, and the reference input equals 100 kHz (0.1 MHz), the VCO output is: $f_o = f_R(NM + A) = 0.1[(200 \times 64) + 10] = 1281$ MHz or 1.281 GHz.

Incrementing the A value provides a change step equal to the reference input

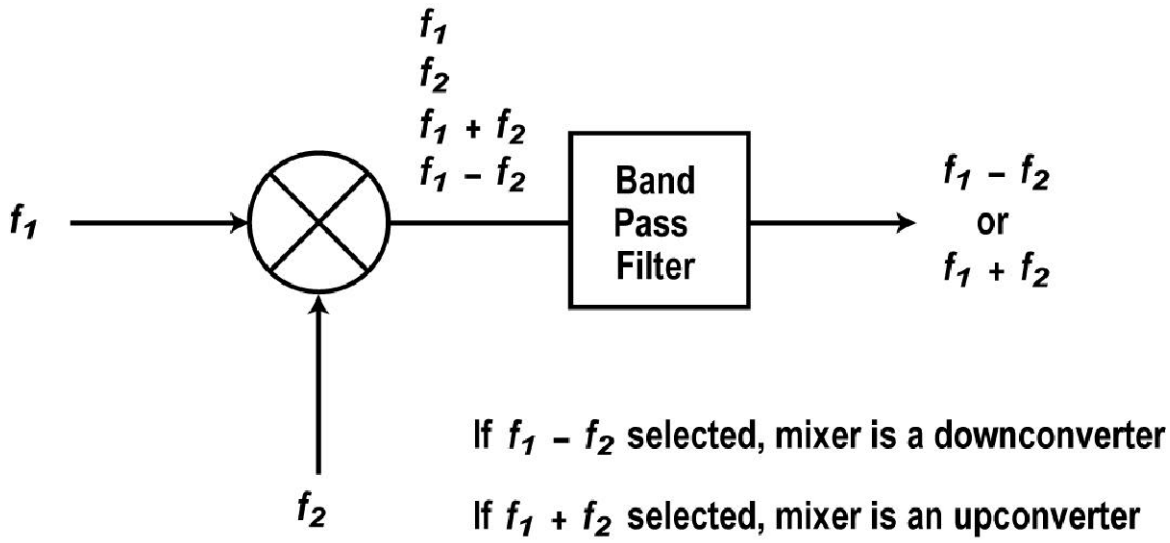
# PLL and Mixers




Phase-locked loop synthesizers are often used with mixers to achieve the desired frequency range of the output.

A mixer is a circuit that has two inputs, $f_1$ and $f_2$, and produces an output that contains $f_1$, $f_2$, $(f_1 + f_2)$ and $(f_1 - f_2)$. A filter is used to select the desired output. The sum and difference signals are those of interest and the difference is the most widely used.

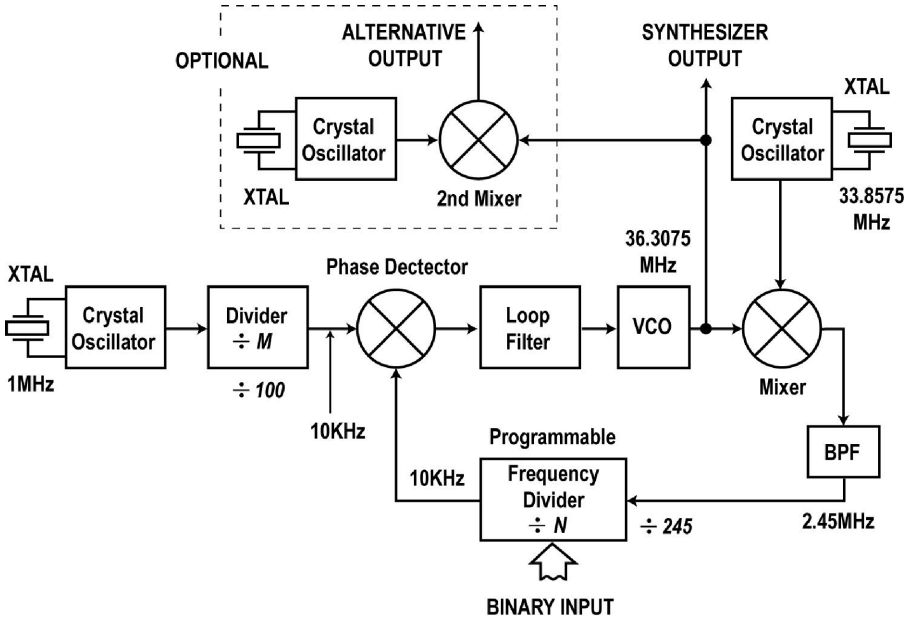
# Example: PLL and Mixers




If a mixer has inputs of 98.7 MHz and 109.4 MHz, the mixer outputs are 208.1 and 10.7 MHz. The 10.7 MHZ is the most useful because it is at a lower frequency.

Mixers whose output is the difference are called downconverters.

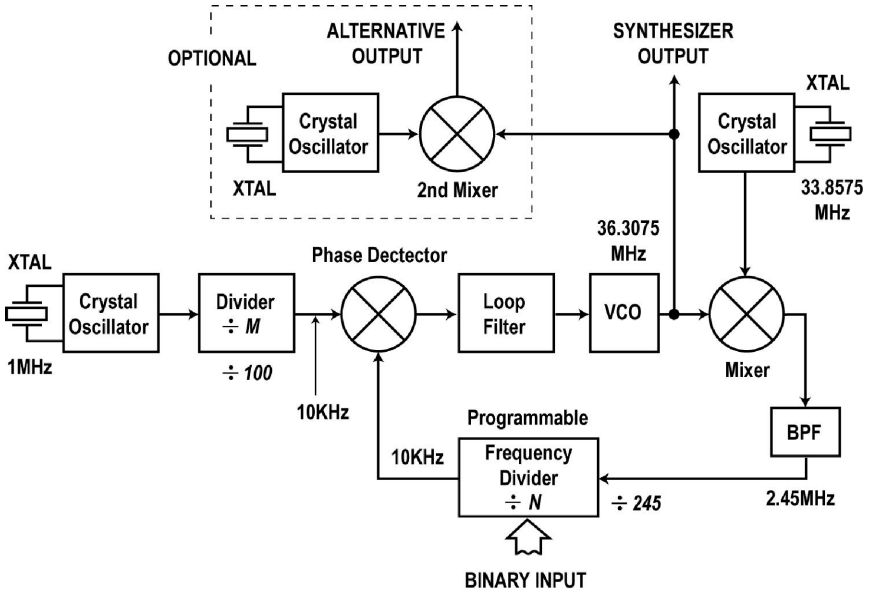
# A Downconverting Mixer PLL




This figure shows a mixer used between the VCO output and the programmable divider input. The mixer inputs are the 36.3075 MHz from the VCO and the output of a crystal oscillator set to 33.8575 MHz. The mixer output is the difference 2.45 MHz.

The programmable divider divides by 245 to produce an output of 10 kHz to the phase detector.

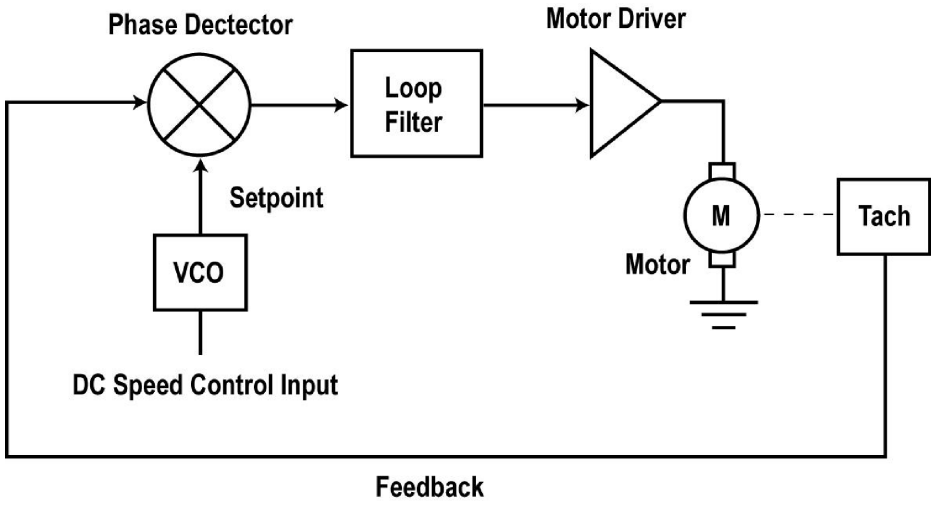
# A Downconverting Mixer PLL




The value of the mixer in this application is twofold. First, it allows the programmable divider to divide by a much lower factor which simplifies the divider. Second, it allows the use of a lower reference frequency. This allows a frequency change increment that is smaller at the higher operating frequency.

A second mixer on the VCO output can also be used to translate the output to some other desired frequency.

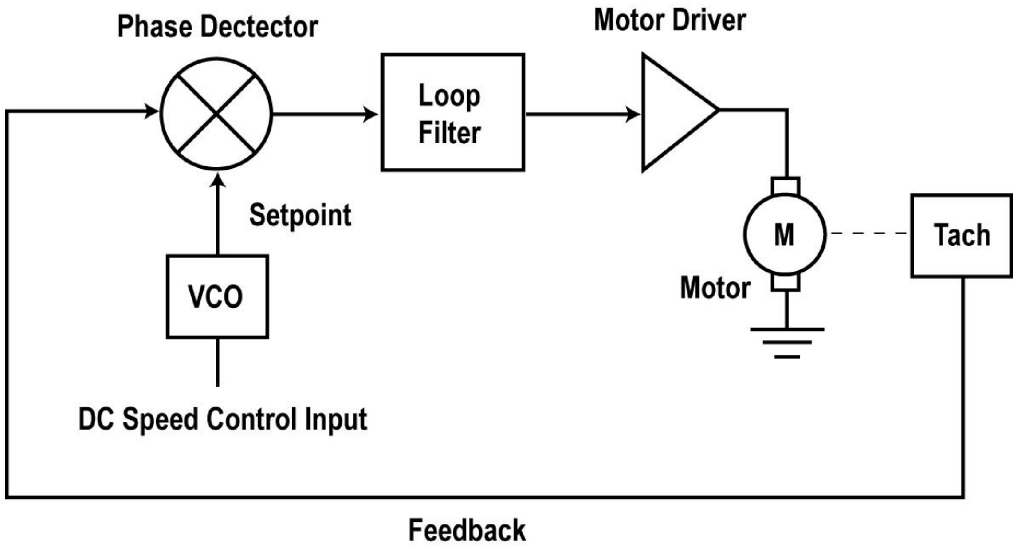
# PLL in Motor Speed Control




A PLL provides a highly precise way to set and control the speed of a motor. The motor may be DC, AC, brushless, stepper, etc. but drive and control methods will vary.

A tachometer (tach) attached to the motor shaft generates a signal whose frequency varies with motor speed. The tach provides a measure of the motor speed in revolutions per minute (rpm). This is the feedback signal in the PLL.

# PLL in Motor Speed Control




The motor and tach essentially replace the VCO in the feedback loop. The tach input is applied to one input of the phase detector.

The other input to the phase detector is from a VCO. A DC control voltage to the VCO input is used to set or adjust the motor speed. The VCO provides a fixed set point input to the system just as a crystal oscillator does in a standard PLL.

# PLL Motor Speed Control

The DC output of the loop filter is amplified in a power driver, using either an amplifier or a switch, to operate the motor.

If the motor speed should change, with a heavier load, the tach output frequency will drop. This frequency will now be less than the VCO set point frequency. This produces an error signal that is filtered and amplified. It is used to increase the drive to the motor which increases the speed to compensate for the original decrease.

The PLL control method is very sensitive and, therefore, provides very precise control of speed in those applications where this is important. Disk drive motor speed in an example.

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# Phase-Locked Loops and Applications Knowledge Probe 2

## Phase-Locked Loop Applications

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