Integrated Nano-Photonics:
The Transition to High-Volume Manufacturing and Implications for Workforce Education

Robert Geer

Professor and PI NSF NEATEC ATE Center

AIM Photonics (Manufacturing USA Institute)

College of Nanoscale Science & Engineering

SUNY Polytechnic Institute

October 17, 2019 The Webinar will begin at 1PM Eastern time

This Webinar will be recorded and we will send you a link

Please use the chat window to ask questions

Complete our brief survey at the end, we want to hear from you

This Webinar Is Hosted By

ATE Central acts as an information Hub for the National Science Foundation ATE Grantee Community

atecentral.net/webinars

This Webinar Is Brought To You By

NACK Network
Building College-University Partnerships for Nanotechnology Workforce Development

NCI Southwest

Introductions

Mike Lesiecki, host

Atilla Ozgur Cakmak, NACK Network

Robert Geer, Professor of Nanoscale Science

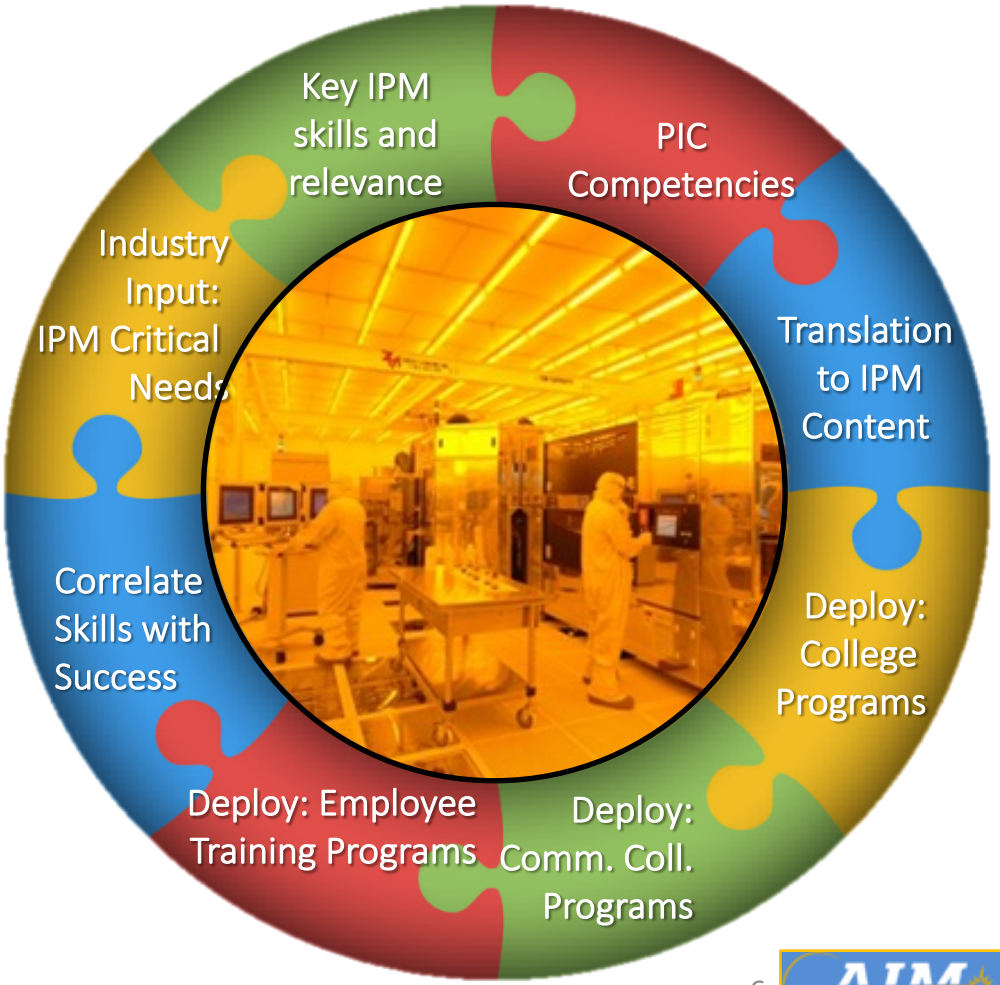
Luka Partners

PennState

SUNY Polytechnic Institute

Outline:

- Integrated Nano-Photonics Manufacturing (**IPM**): Overview & comparison with ICs
- Photonic Integrated Circuits (**PIC**s) – Turning the corner on high-volume manufacturing
  - Key manufacturing advances
  - Design ecosystem
  - Foundry model
- Skills and Tasks for IPM Technicians
  - PICs vs ICs
  - Assembly & Test
  - Packaging
- Tech Education Modules
  - PIC Testing
  - PIC Wafer-scale/Chip-Scale QC
  - Advanced Packaging (2.5D/3D Assembly)

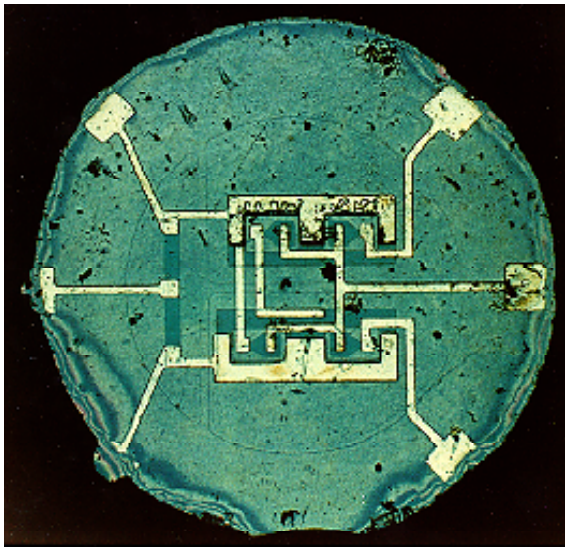


Before Getting to Integrated Nano-Photonics Manufacturing…

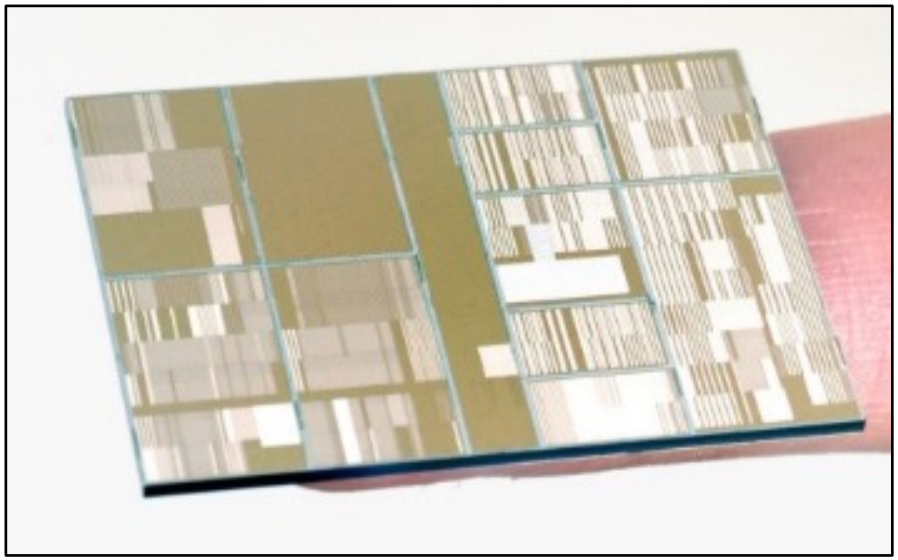
A Little History on Integrated Circuits

Historical Perspective – Integrated Circuits

- 1961 and 2018 integrated circuits.
- Progress due to:
  - **Feature size reduction - 0.7X/3 years (Moore's Law)**
  - **New Materials – conductors, dielectrics, semiconductors**
  - **New Devices/Designs – FinFETs, AI-specific designs**

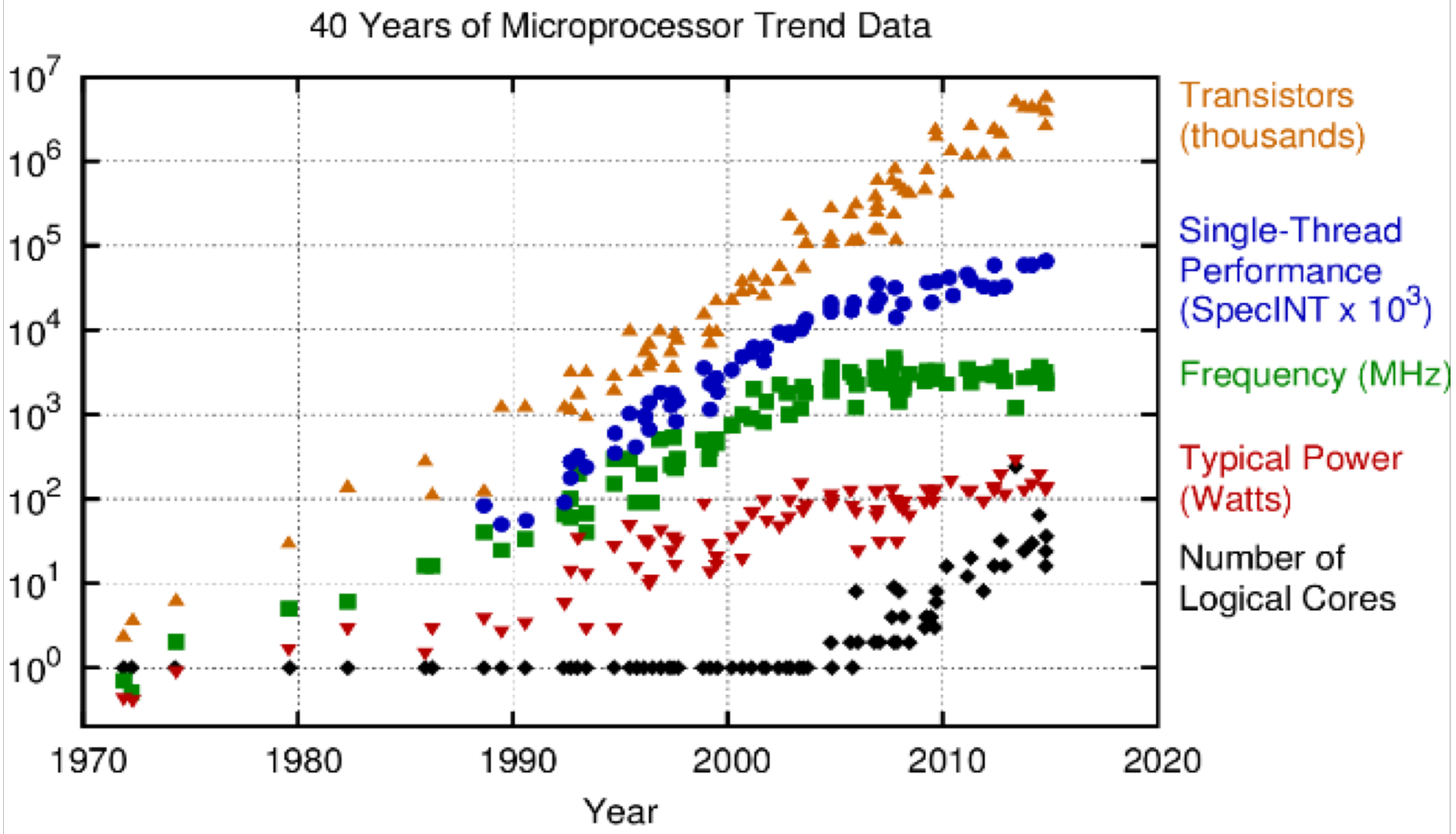


First Planar Integrated Circuit 1961:
4 Transistor Flip-Flop



IBM 7nm Node Chip 2018:
20 Billion Transistors

Historical Perspective – IC-Enabled Systems



I7-980x: image from http://www.computershopper.com/components/reviews/intel-core-i7-980x-extreme-edition
First Integrated circuit image: https://en.wikipedia.org/wiki/Jack_Kilby#/media/File:Kilby_solid_circuit.jpg

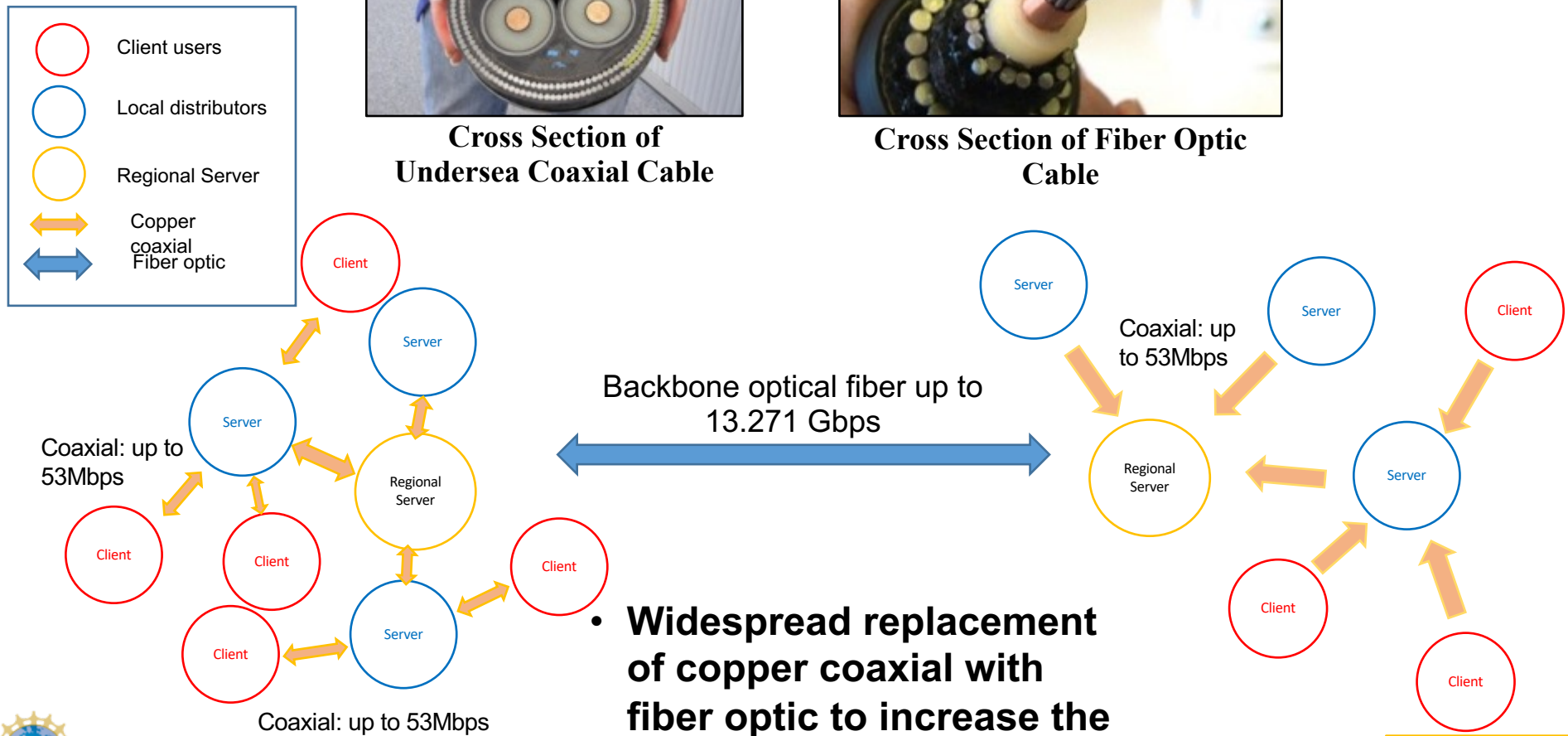
And then there's photonics…

"The physical science of light (photon) generation, detection, and manipulation through emission, transmission, modulation, signal processing, switching, amplification, and sensing."

Fiber Optics – Revolutionizing Communication

Cross Section of Undersea Coaxial Cable

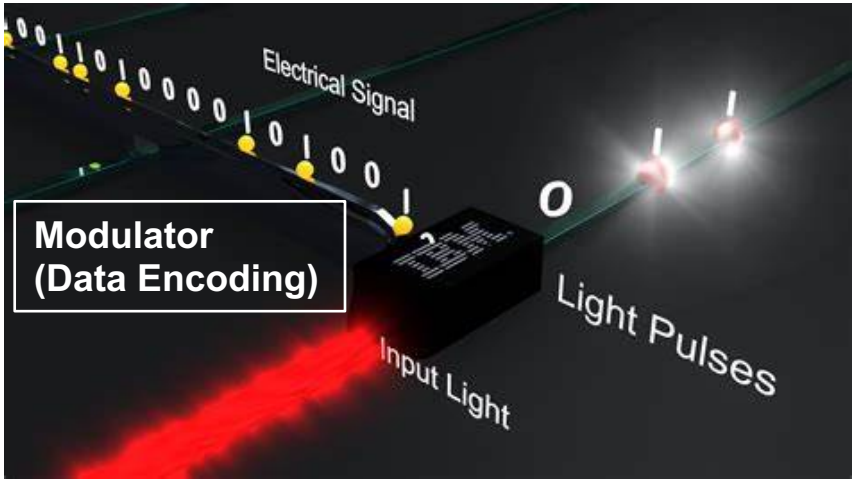
Cross Section of Fiber Optic Cable

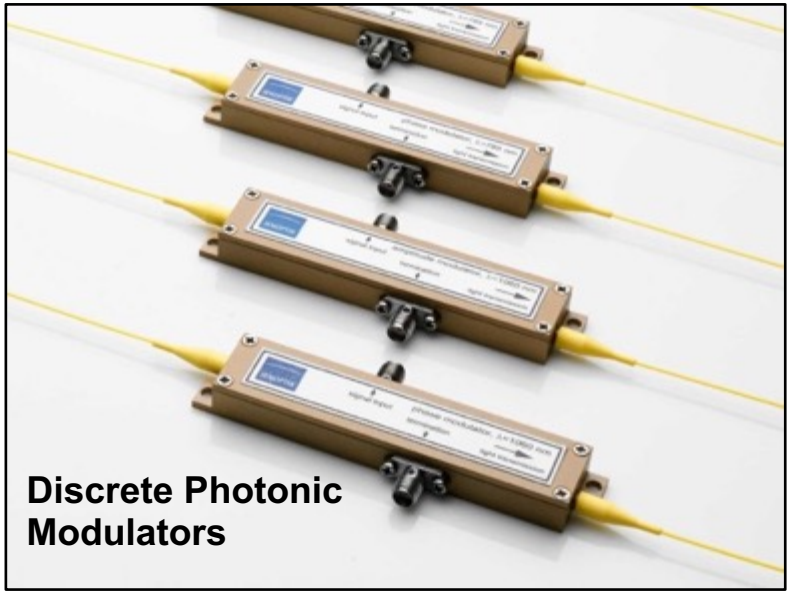


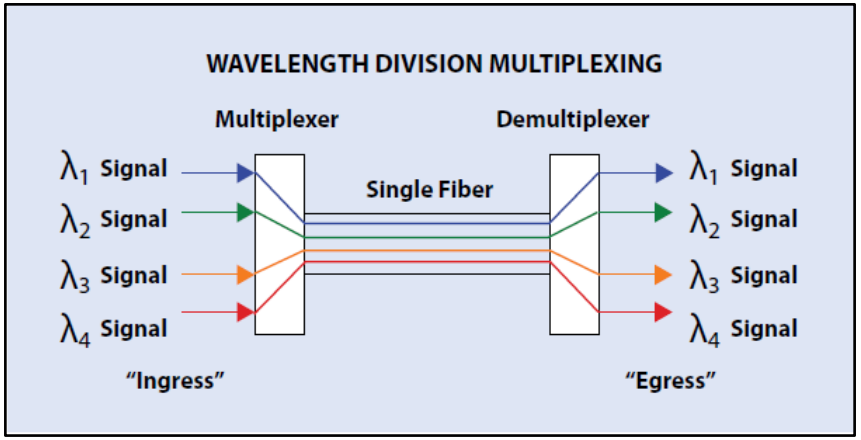
- **Widespread replacement of copper coaxial with fiber optic to increase the data transfer**

Photonics Systems – Driven by Discrete Components

- In telecommunications discrete photonics components have dramatically increased data transmission
  - Sources (infra-red lasers)
  - Interconnects (fibers)
  - Detectors (PIN diodes)
  - Encoders (modulators)







- Wavelength division multiplexing dramatically increases data rates

Integrated Photonics – Sources, Devices, and Detectors on a Single Chip

But First a Poll Question

What is the difference between Photonics and Integrated Nano-Photonics?

a) Integrated Nano-Photonics refer to photonic devices integrated on a single chip.
b) Integrated Nano-Photonics don't include waveguides or fiber optics.
c) Integrated Nano-Photonics always include transistors.

Another Poll Question

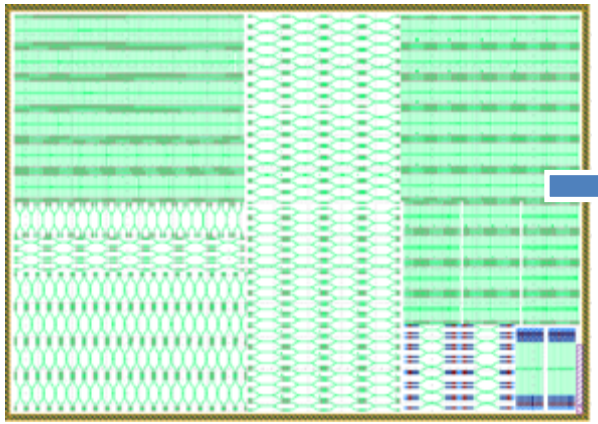
In the context of Integrated Nano-Photonics what does PIC stand for?

a) Abbreviation for ‘Picture’

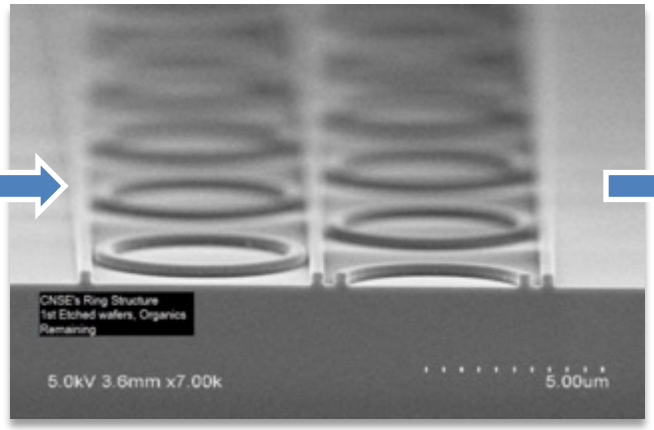
b) Abbreviation for ‘Photonic Integrated Circuit’

c) Abbreviation for ‘Positive Index Contrast’

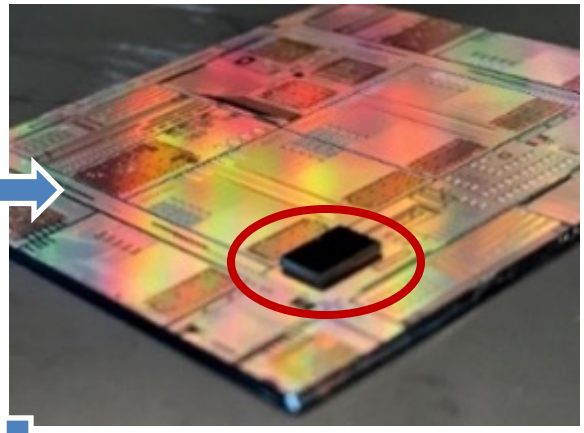
Adapt Si-based IC Methodology to Integrate Photonics Components



Photonic device & interconnect design and layout

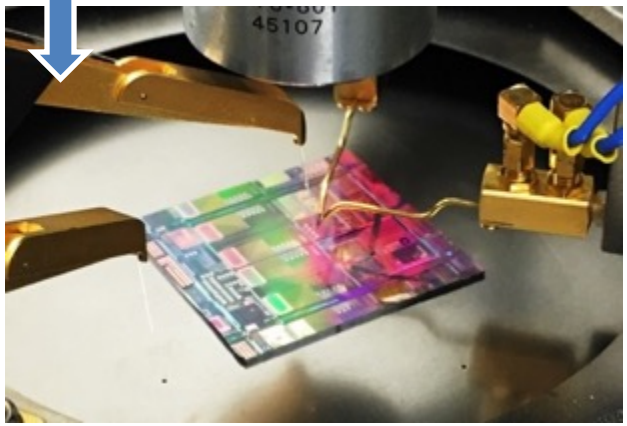


Fabrication of Si-based photonic devices (SEM of Si modulator)



Photonic Integrated Circuit (PIC) (with laser attached)

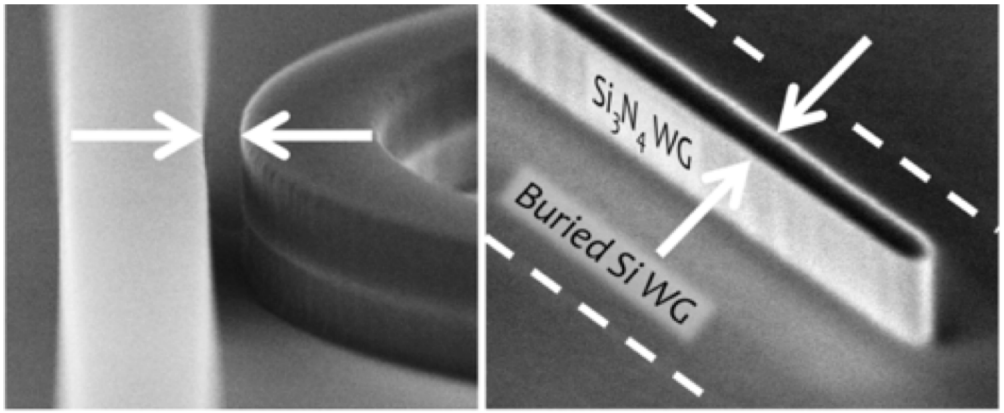
- Photonic Integrated Circuits (PICs) combine:
  - On-chip Si waveguides (e.g. fibers)
  - Devices (e.g. modulators)
  - Light sources (lasers)
  - I/O structures



Electro Optical test of PIC chip

PICs: Transition to High-Volume Manufacturing (HVM)

- Why now?
  - Key Manufacturing Advance: Lithography
  - PICs not practical before 193nm immersion litho



95nm gap in Si. 95nm Si3N4 taper on Si waveguide.

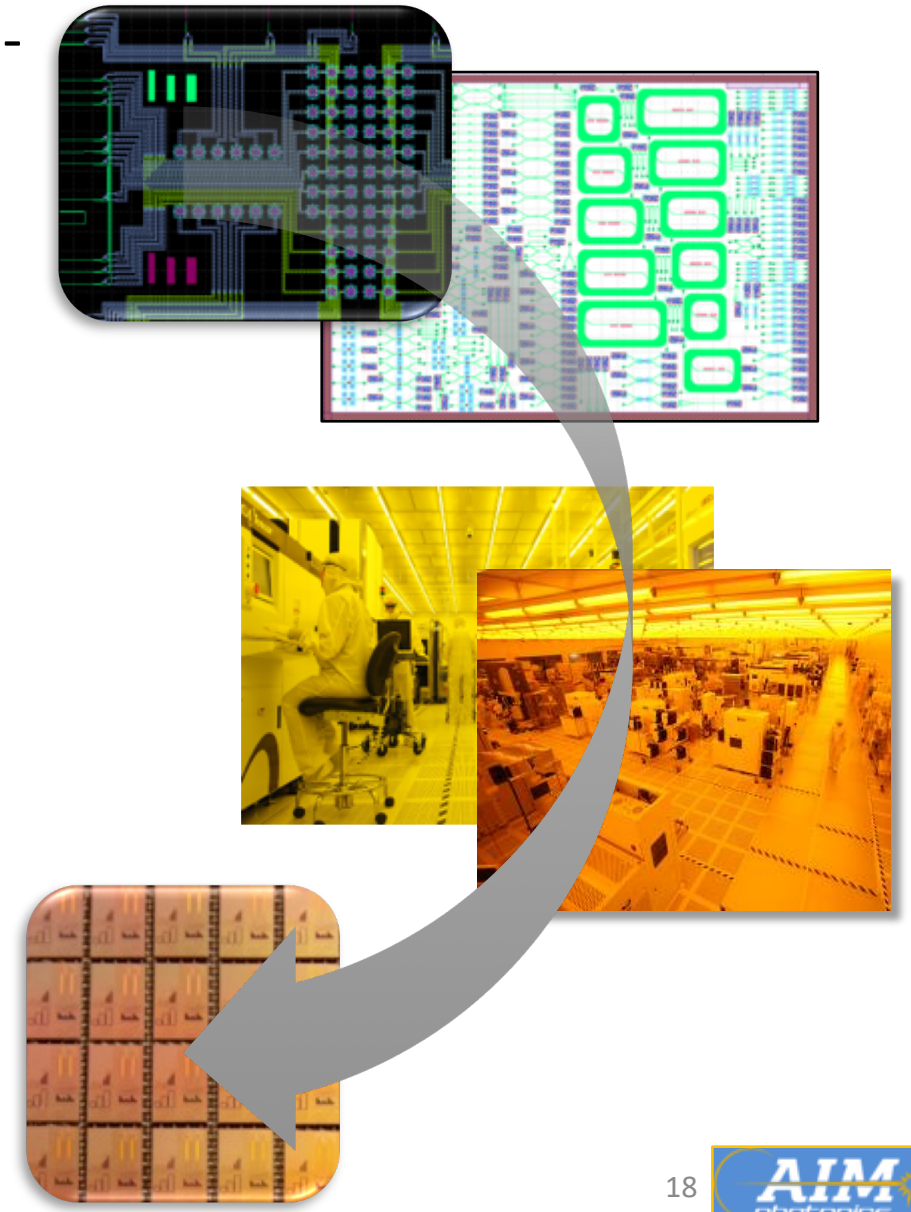
TWINSCAN NXE:3300B
Photo: www.asml.com

TWINSCAN NXT:1950i
193-nm Step & Scan
Photo: *ww.asml.com*

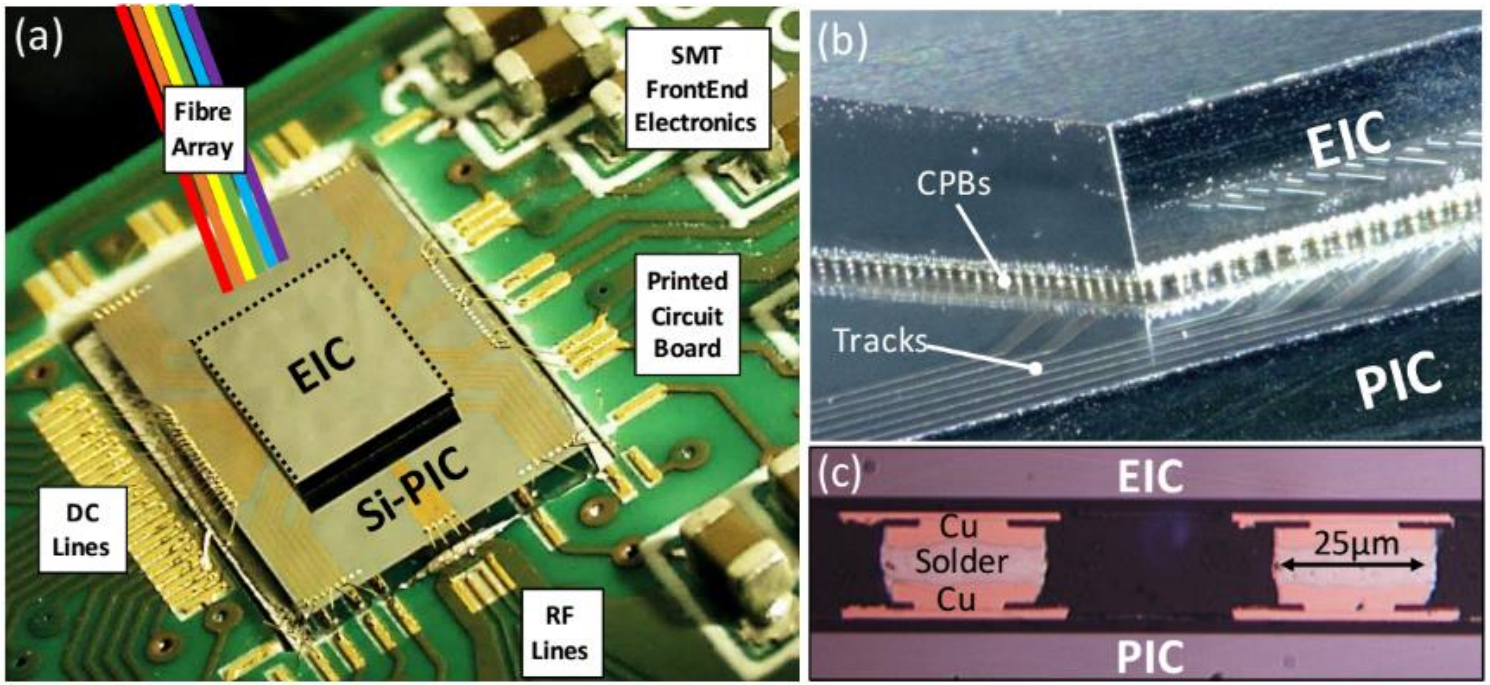
	Tool type	Dense L/S (1:1)	Isolated Line	Dense Via
EUV	ASML 3300B	18nm	16nm	25nm
193nm	ASML 1950i	42 nm	35 nm	60 nm
Immersion	ASML 1700i	50 nm	40 nm	70 nm

HVM: Establishing the PIC Ecosystem through

- Electronic and photonic design/co-design – Requires CAD infrastructure
  - Enables widespread PIC design workforce
  - Allows designers to build on established IP
- Full 300mm wafer fabrication and test infrastructure (wafer & die)
  - Rapid prototyping and optimization
  - 'Foundry' model to enable broad adoption of PIC solutions
- Interposers & chip attach
  - Integration with IC's
  - Laser attachment and packaging



HVM: Integrating PICs with ICs



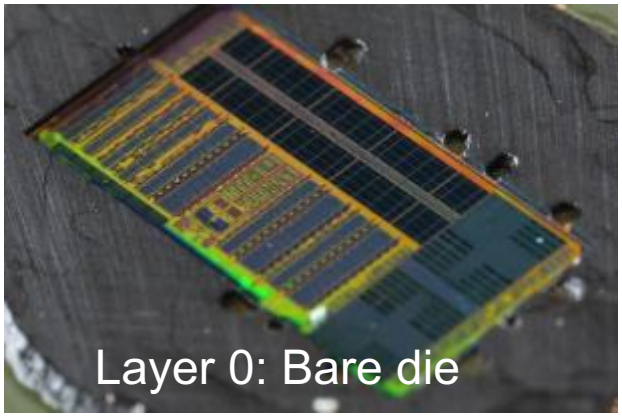
<u>Vertical integration of an electronic IC (EIC) driver-chip on top of a Si-PIC</u>

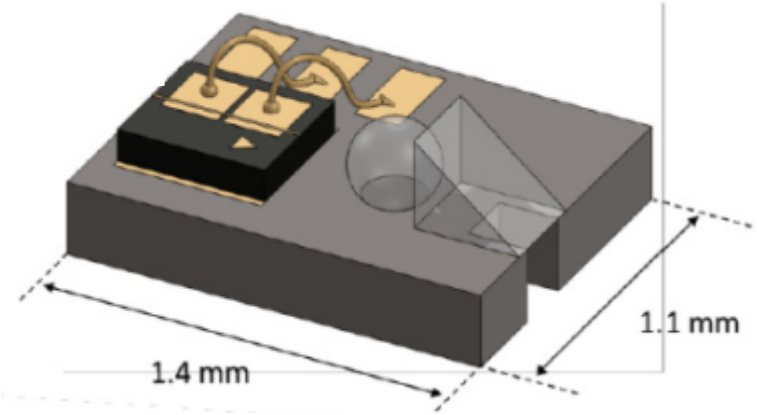
(**a**) EIC integrated on a PIC, with RF (radio frequency) and DC (direct current) signals routed from front-end electronics on the PCB

(**b**) EIC integrated onto the PIC using discrete copper-pillar-bumps (CPBs)

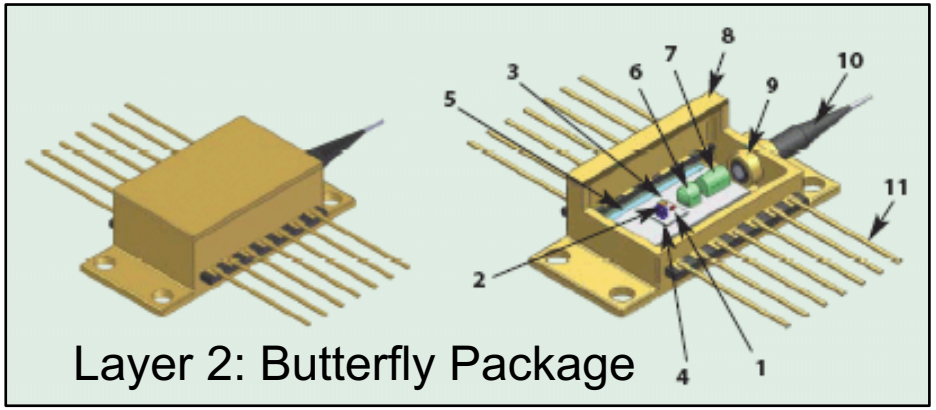
(**c**) Image of interconnects between the EIC and PIC.

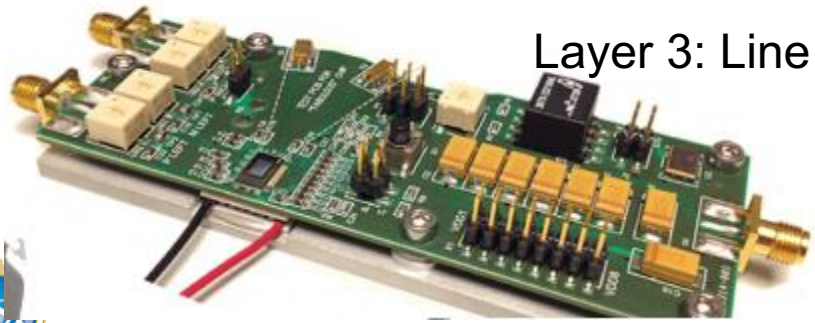
HVM: From PIC Fabrication to Packaging & Systems





Layer 1: Micro-Optic Bench





Layer 3: Line Card

Layer 4: Photonics Rack

Source: 6

Poll

Which statement is true about Integrated Nano-Photonics?

a) Integrated Nano-Photonics products won't be introduced to the market until the next decade.

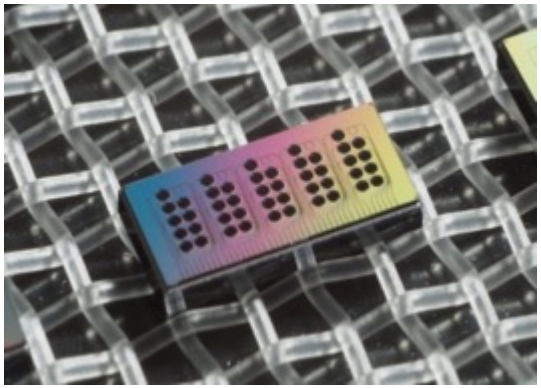
b) Integrated Nano-Photonics products are in the market now.

c) It is unlikely that Integrated Nano-Photonics products will ever make it to market.

Key PIC Technologies

PIC Sensors

- Improved healthcare
- Threat mitigation
- Spectroscopy
- Low cost and disposable



Microfluidics to enable real-time detection of biological substances such as protein biomarkers of human stress and traumatic brain injury.

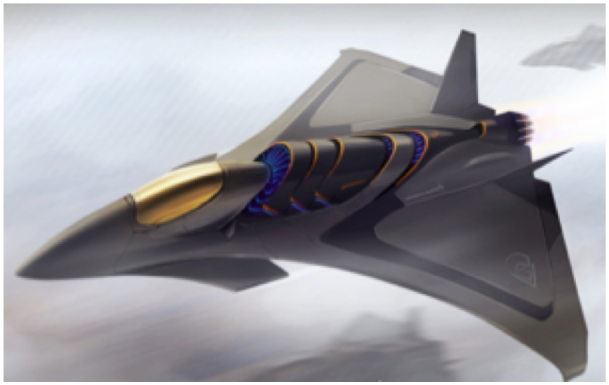
Data Comm / Telecom

- Connect the world
- More energy efficient
- 400Gbs, 800Gbs, 2.56Tbs
- Protect the environment

Increase performance of server farms while decreasing energy consumption and simultaneously expanding global communication.

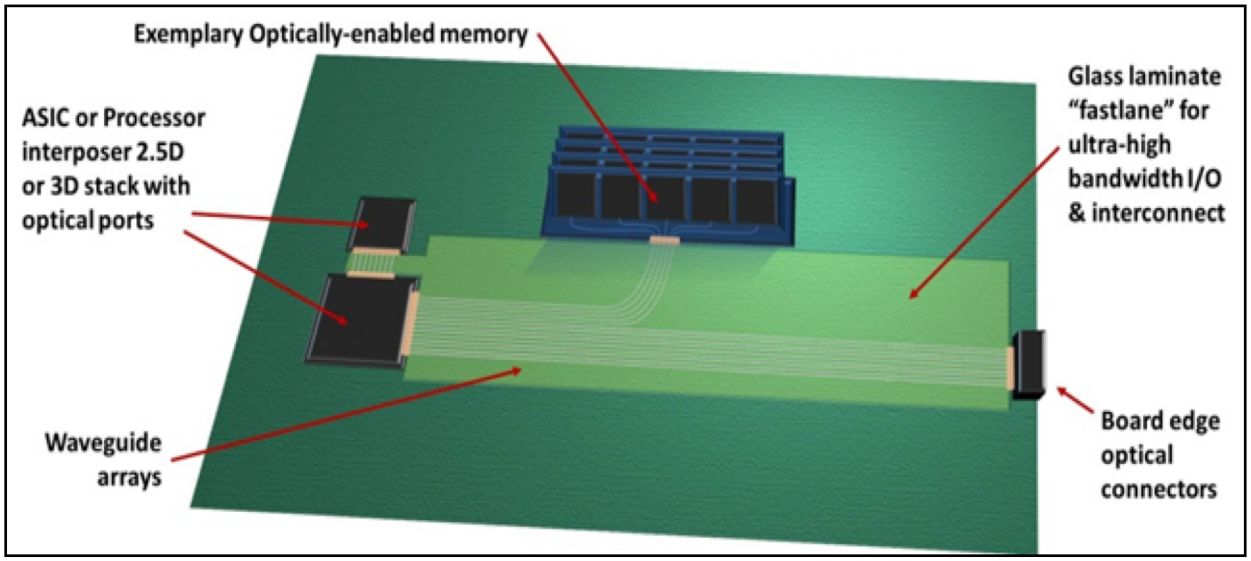
RF over Fiber

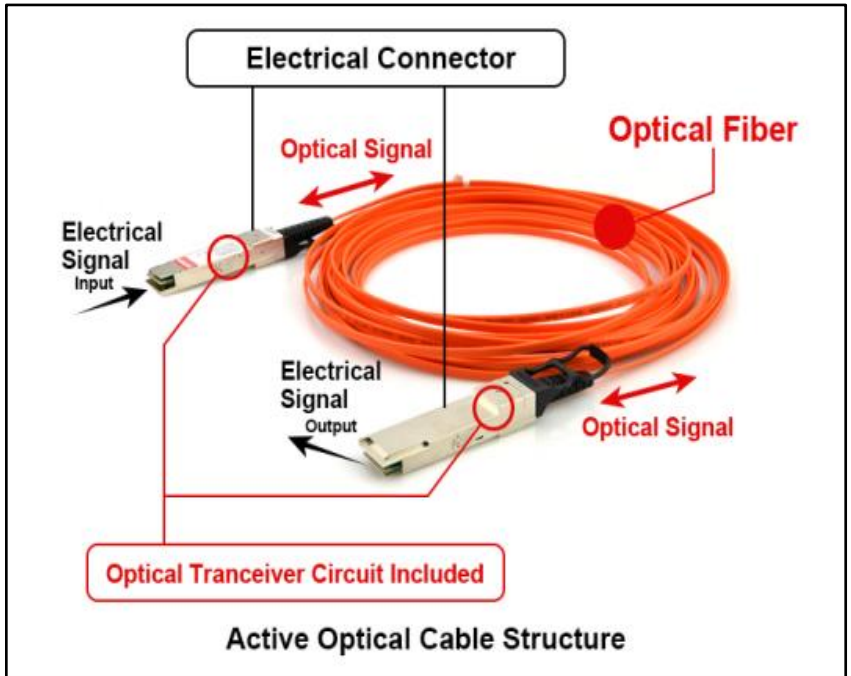
- Lighter, faster, less power required
- More compact and cost effective
- Multiple sources of info in one fiber
- Quick adaptability to requirements



With fiber optic cabling, users can add other optical wavelengths resulting in multiple sources of information on one fiber which allows much quicker reaction to changes in environment and requirements.

PIC Technologies in the Market





Questions on PIC & IPM Intro and Overview?

Integrated Nano-Photonics Manufacturing (IPM): Workforce Skills & Competencies

IPM: Workforce Implications

R&D ➔ Product

IPM Manufacturing Path	Workforce Education Prep
• R&D	B.S./M.S./Ph.D.
• PIC Design & Sim	B.S./M.S./Ph.D. ➔ A.S/A.A.S.?
• PIC Manufacturing	A.A.S./B.S. (some M.S./Ph.D)
• PIC Assembly (KGD Test)	A.A.S./B.S.
• PIC Packaging	A.A.S. (some B.S.)
• Testing/Quality Control	A.A.S.

Increased Task Specialization

- Dominated by 2-yr degrees
- Substantial Overlap with IC Techs
- Some Overlap with IC Techs and Photonics Techs
- Substantial Overlap with Photonics Techs

Manufacturing Technician Skills and Tasks: PICs vs ICs

A Semiconductor Manufacturing Technician Knows:	Knowledge and Skills Needed as an IPM Technician
• The semiconductor manufacturing process (Si-ICs) • Automated materials handling systems (mechanical/electrical components) • Automated fabrication systems (fluid power, PLCs, robotics) • Cleanroom protocols • Vacuum and RF technology • Metrology, SPC, and quality control • Data Integrity, encryption and data security	• Light sources (lasers) particularly VCSELs • Waveguides and waveguide loss measurements • Detectors and detector response measurements • Basic optical characterization • Electro-optic characterization of PICs • Interposer assembly • IC attachment (3D stacking) • PIC and interposer packaging • Fiber attach • Testing and reliability

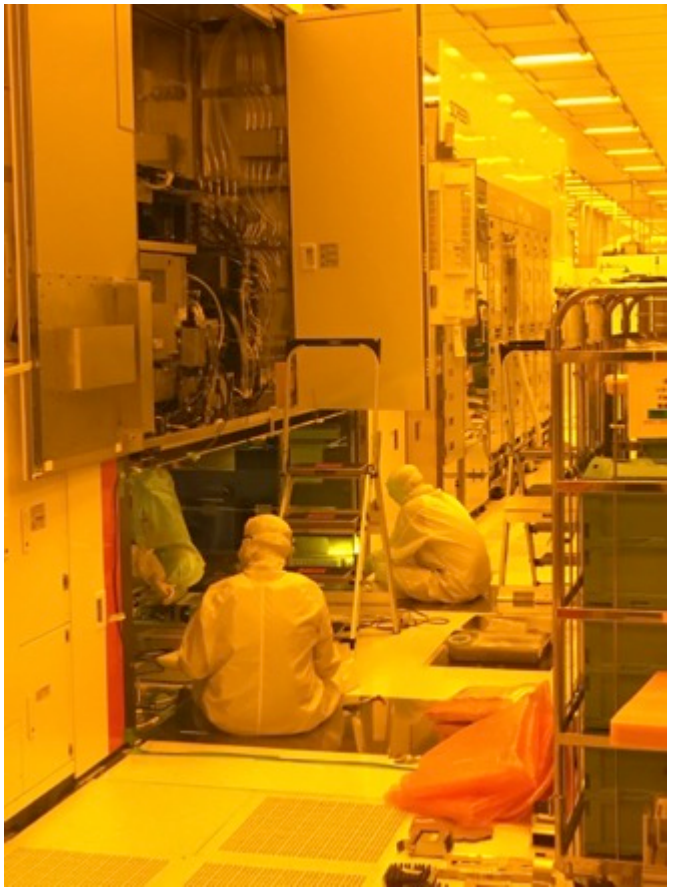
PIC Testing and Specialized Assembly/Packaging

Types of IPM Technicians: First Pass Skills Analysis

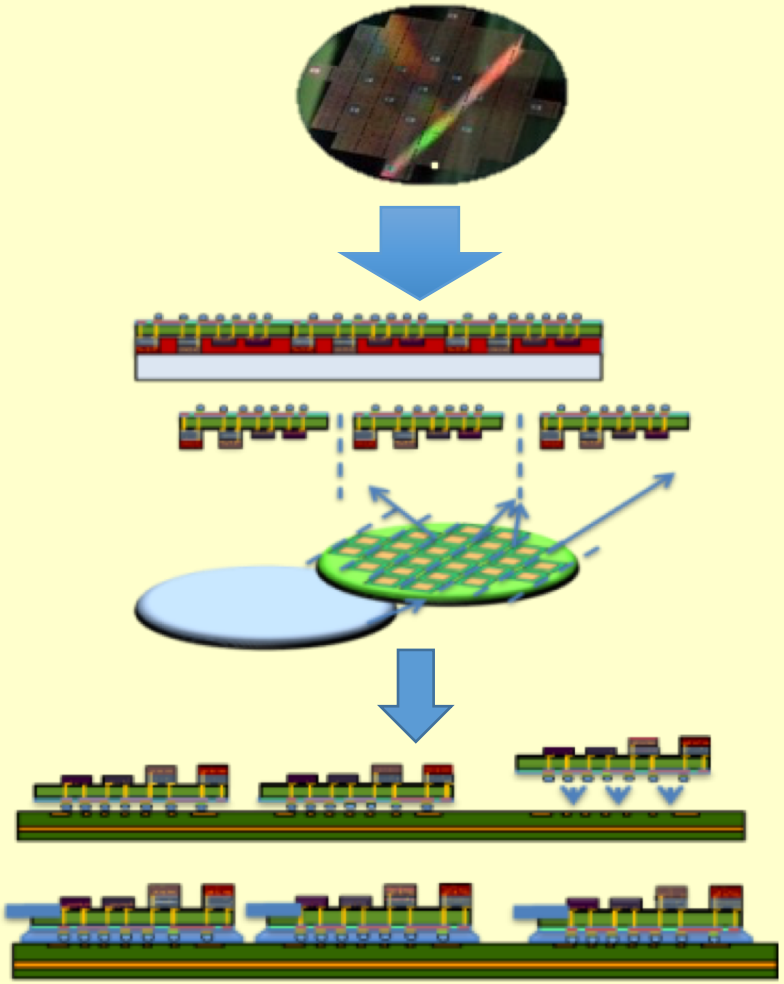
- **"Fab" Equipment Technician**
  - Maintenance, troubleshooting, upgrades and installations of vacuum and cleanroom equipment.
  - Maintenance, troubleshooting, upgrades and installation of automated processing, control and transportation equipment.
  - Nanotech equipment maintenance and operation.
- **Integrated Photonics Test, Assembly & Packaging Techs**
  - Operation and maintenance of equipment to test PIC wafers; interpret results
  - PIC assembly (die to interposer/laser attach/IC to interposer attach)
  - Operation and maintenance of equipment to test PIC assemblies (die-interposer) and interpret results
  - PIC packaging (PCB-level package, fiber attach, sensor package)
  - Operation and maintenance of equipment to test packaged systems

High Overlap w IC Techs

High Overlap w Phot Techs



IPM Test, Assembly and Packaging

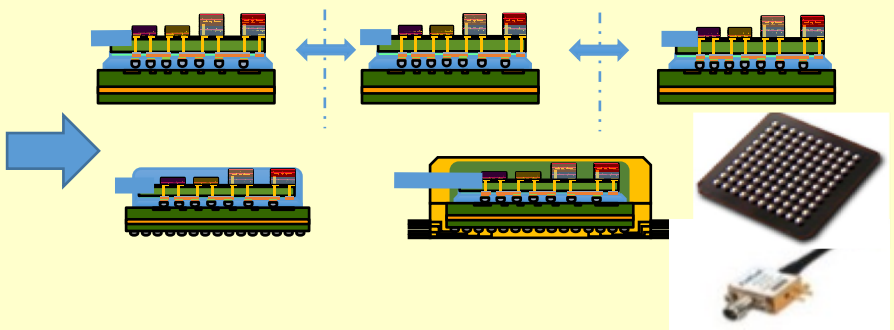


***Wafer-scale* Photonics Packaging**

- Wafer-scale testing *(Opt/RF/DC)*
- PIC & Interposer Metallization
- Die bonding *(laser & PIC)*
- Singulation of die

***Chip-scale* Test, Assembly and Packaging**

- Chip Scale Testing *(Opt/RF/DC)*
- Fiber and Laminate attach
- Surface Mount Assembly



Examples of Critical Work Functions for IPM Test, Assembly & Packaging Techs (Chip-Scale)

1. Clean, Mount, Inspect & Prepare PIC chips for Testing
2. Operate, maintain, and calibrate instrumentation to test PIC chips
3. Conduct tests of PICs, record data, interpret & report results once die is mounted and connected to test station.
4. **PIC Alignment, Assembly, and Packaging**
   a. ***2D, 2.5D and 3D Alignment and Assembly of PICs***
   b. ***Assemble and package PIC stacks into workable IP components***
5. Prepare and connect component packages for testing.
6. Operate, maintain, modify, calibrate, troubleshoot and repair instrumentation to test assembled components.
7. Conduct tests of assembled components, record data, interpret and report results.
8. Conduct long-term system performance testing and failure analysis.

Critical Work Function #4a for IP Test/Assembly Techs

2D, 2.5D and 3D Alignment and Assembly of PICs.

Task A

Alignment and 3D Bonding of ASIC die on PIC die

- Operate micro-optic pick/place equipment for ASIC or memory die on PIC die
- Perform bonding/attachment and/or under-fill between die

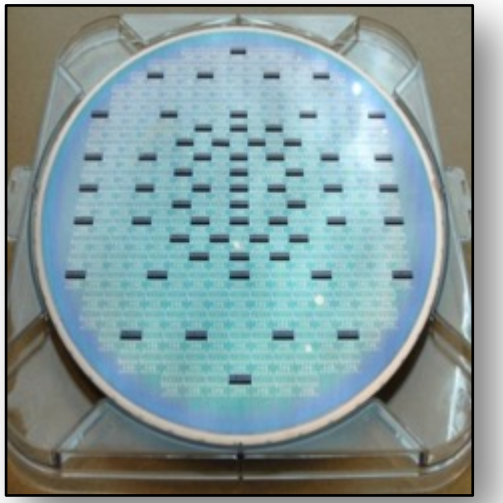
Task B

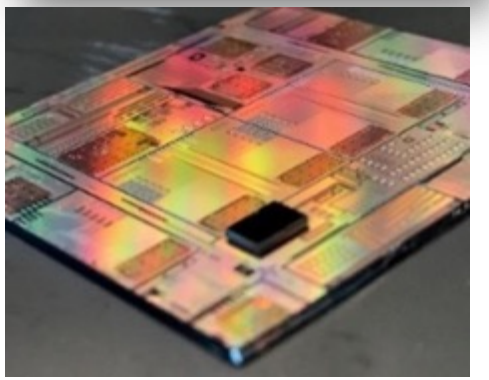
Alignment and Bonding of various die on passive or active interposer.

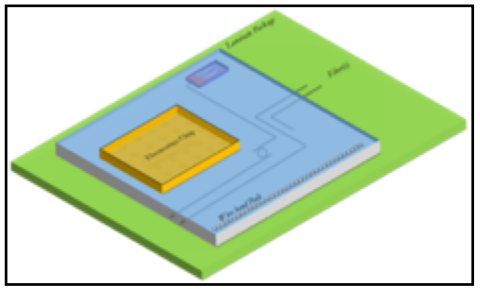
- Operate micro-optic pick/place equipment for PIC die on passive or active interposer
- Operate micro-optic pick/place equipment for ASIC or memory die on passive or active interposer
- Operate micro-optic pick/place equipment for IR laser sources on passive or active interposer
- Perform bonding/attachment and/or under-fill between die and interposer

Task C

3D inspection of full die stack or die/interposer stack.







Critical Work Function #4b for IP Test/Assembly Techs

Assemble and package PIC stacks into workable IP components.

Task A - Place PIC interposers into optical package.

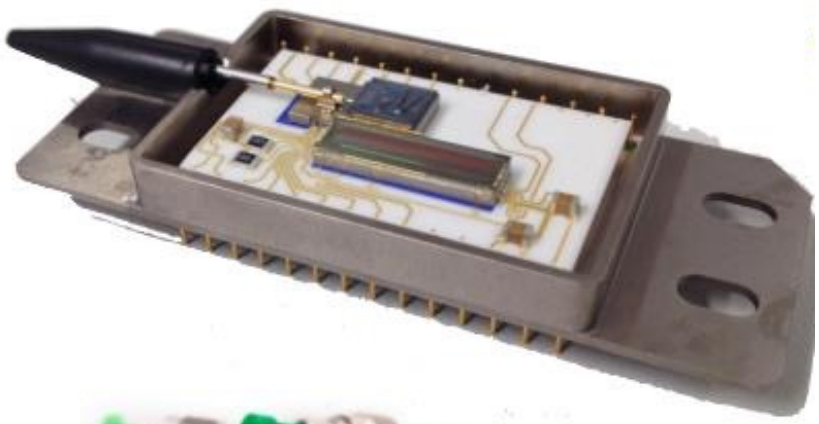
Task B - Setup components for precision alignment.

Task C - Wire bonding for electrical control signals.

Task D - Create optical fiber connections.

Task E - 3D inspection of fiber alignment/connection.

Task F - Verify final package connection integrity and troubleshoot as needed.



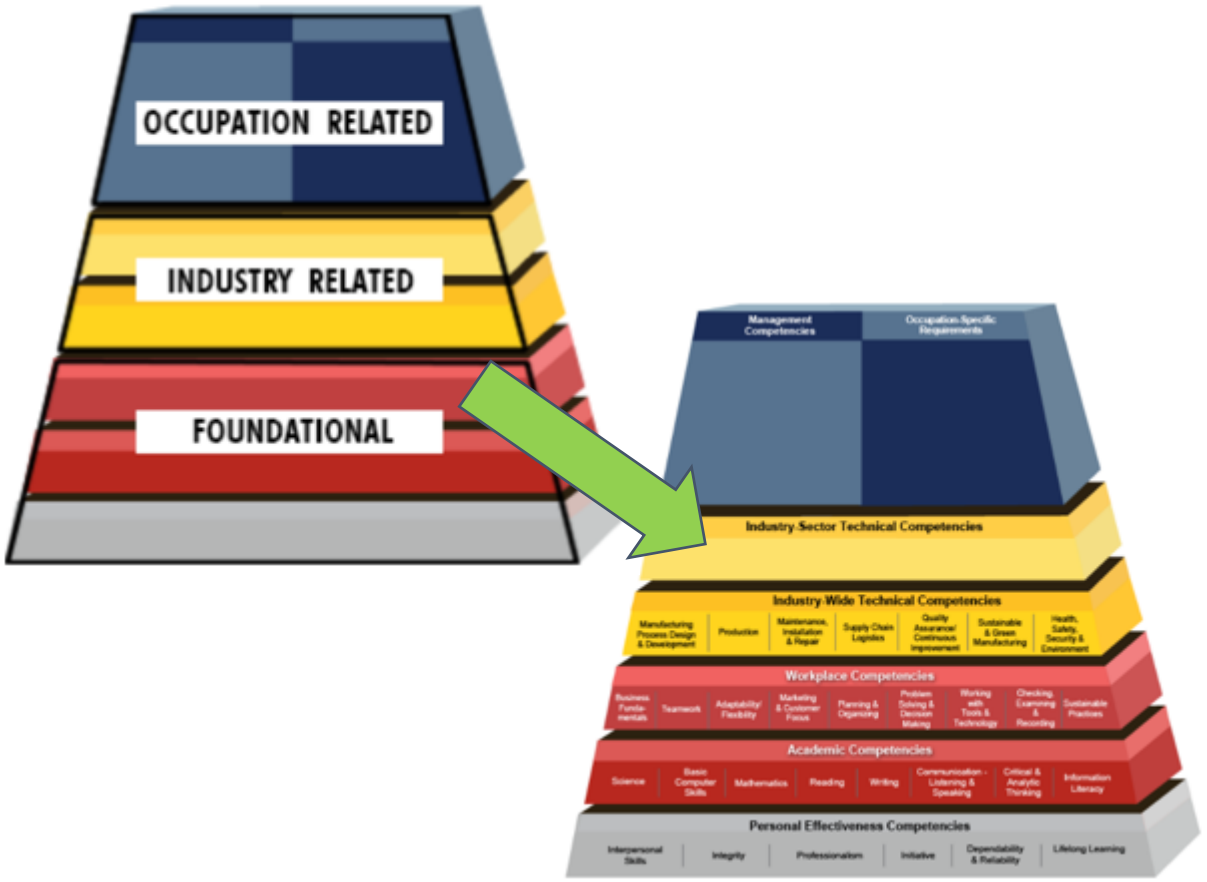
Where do IPM Tech Skills Fit?

IPM Educational Module Design: Technician Competency Model

- Basic DOL Technician Competency Blueprint:

  IPM program focused on mid-range tiers: 4-6

Tier Definitions for Technician Training Competency Model	
Occupation Related	
Tier 9	Management Competencies
Tier 8	Occupation-Specific Requirements
Tier 7	Occupation-Specific Technical Competencies
Tier 6	Occupation-Specific Knowledge Competencies
Industry Related	
Tier 5	Industry-Specific Technical Competencies
Tier 4	Industry-Wide Technical Competencies
Foundational Competencies	
Tier 3	Workplace Competencies
Tier 2	Academic Competencies
Tier 1	Personal Effectiveness



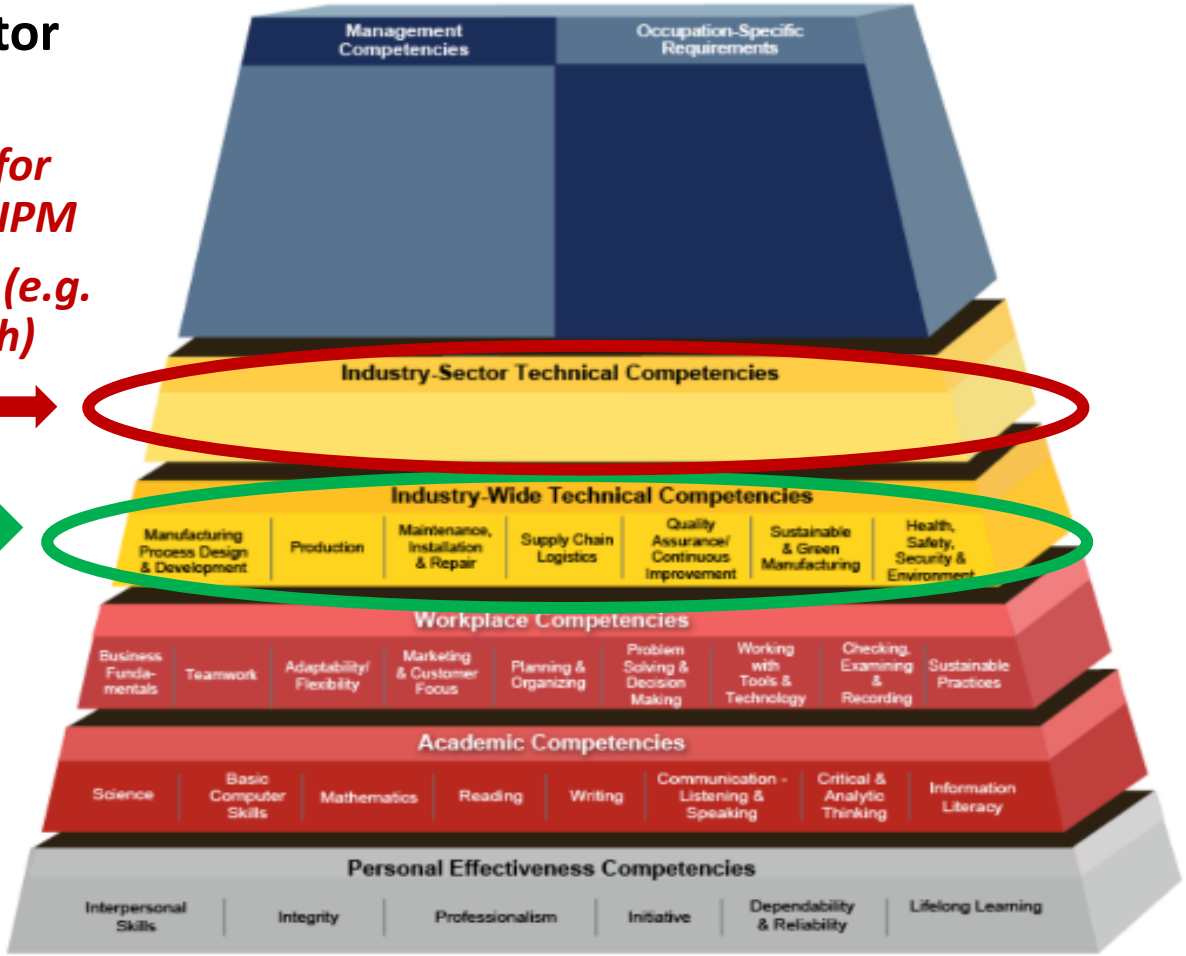
Competency Model Template (US DOL)

<u>Industry Sector:</u> Semiconductor Manufacturing and IPM

- ***Previously undeveloped for Semiconductor Mfg and IPM***
- ***Build on existing models (e.g. MATEC & SEMI/Sematech)***

<u>Industry-wide:</u> Advanced Manufacturing

- **Sufficient foundational skills?**
- **Data literacy?**
- **Intro to 'Design Concepts'?**



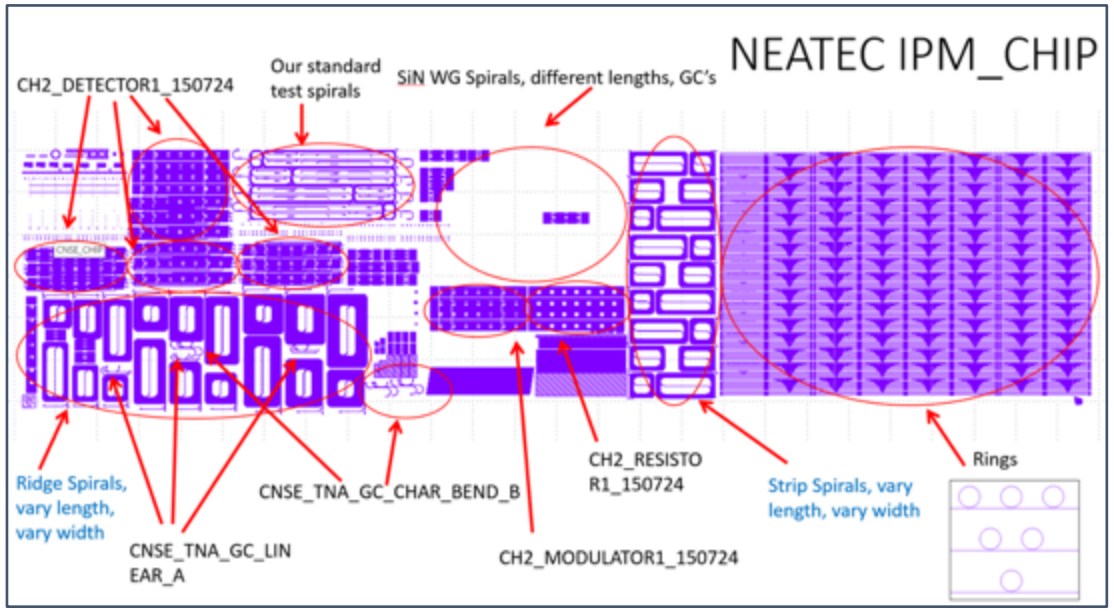
Questions on PIC & IPM Tech Skills?

IPM Tech Education Module Design: Course/Module Tier Designations

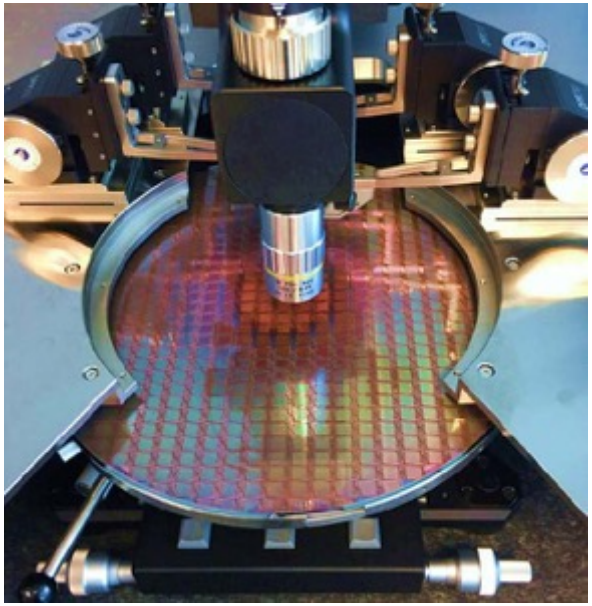
- IPM Course Elements and Technician Competency Tier

IPM Modules	Technician Competency Tier
1. **General IPM technology overview modules:** *e.g. basic IPM concepts and IPM applications*	**Tier 2**
2. **Process basics 1:** *Underlying topics and skills associated with the base IP fab process*	**Tier 4**
3. **Process basics 2:** *compound process basics that combine multiple capabilities and skills*	**Tier 4**
4. **Specific manufacturing process flow and systems modules:** *e.g. Si-based IP manufacturing process flow and key IP processing modules*	**Tier 5**
5. **Assembly, metrology/test, and quality control modules:** *e.g. 2.5D/3D IP assembly, basic performance testing of on-chip IP devices, etc…*	**Tier 5**
6. **Practical training courses (Internships, capstone experiences at IPM-equipped facilities):** *e.g. 300mm Si fabrication cleanroom process operator internship (currently in place at SUNY Poly)*	**Tier 6**

IPM Technician Test Chip for IPM Technician Education Modules

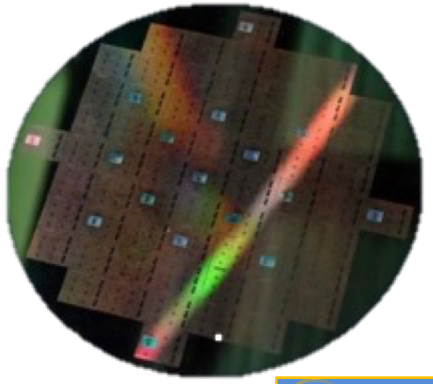


Non-proprietary IPM test structures (SUNY Poly)



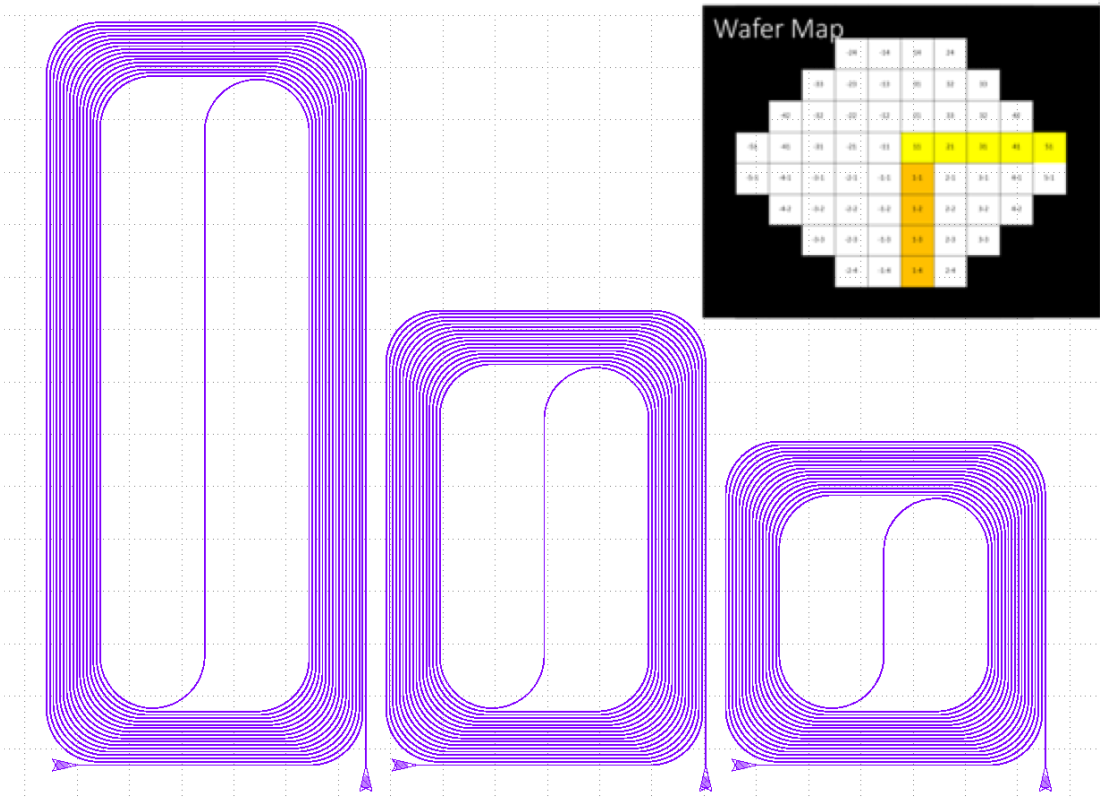
IP wafer on NEATEC test station

- Passive test structure development (Chipsets #1) development/fab completed
- Designed for use with NEATEC test station in NEATEC user facility



NEATEC IPM: Technician Task Example

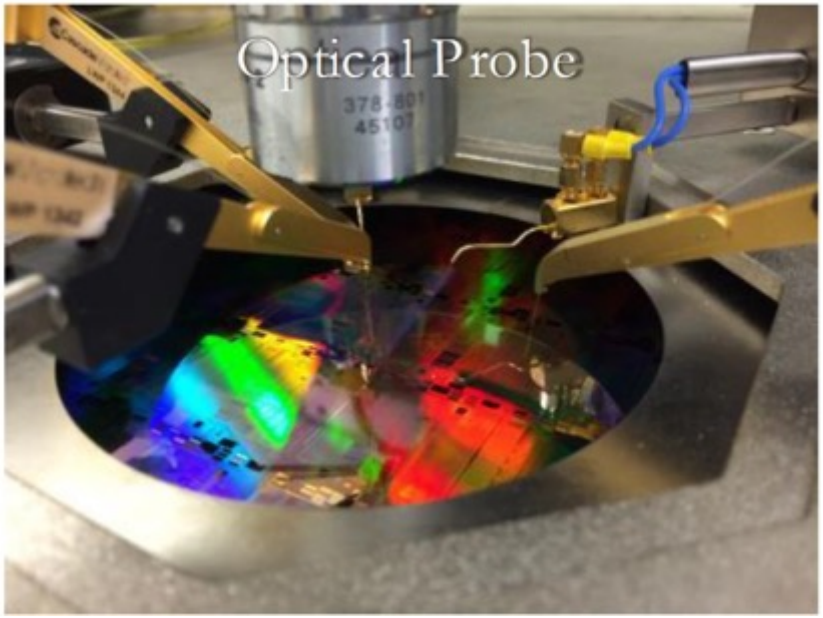
- **Technician Task:** **'Cut-back' loss measurement for on-chip waveguides. Determine optical loss (dB/cm) and compare with design spec**
- **Key Skills:**
  - **Die/wafer place**
  - **Probe align**
  - **Data acquisition**
  - **Collate/document**
- **Hands-on element for:**
  - ***Wafer-scale PIC Testing***
  - ***Chip-scale PIC Testing***

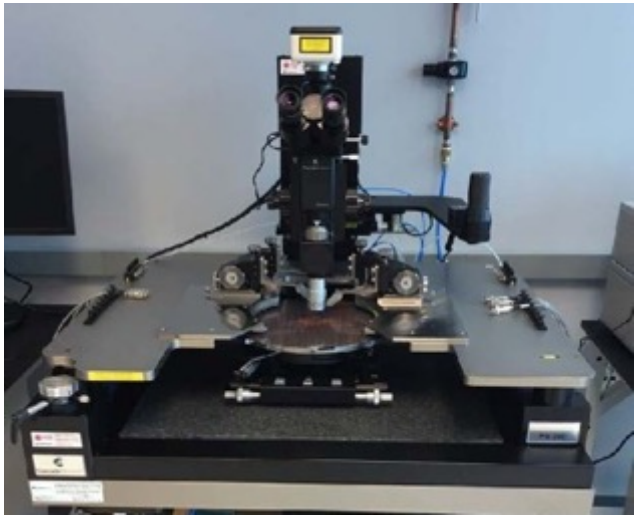


5cm spiral on-chip waveguide **3cm spiral on-chip waveguide** **2cm spiral on-chip waveguide**

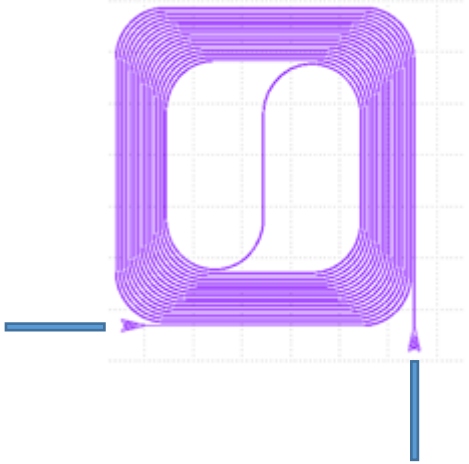
IPM: Technician Skill – Probe alignment

- **Skill Example: Probe Align**
  - **Probe align for Si waveguide measurement (loss)**
  - **Probe configuration**
  - **Power optimization**
- **Hands-on element for:**
  - ***Wafer-scale PIC Testing***
  - ***Chip-scale PIC Testing***

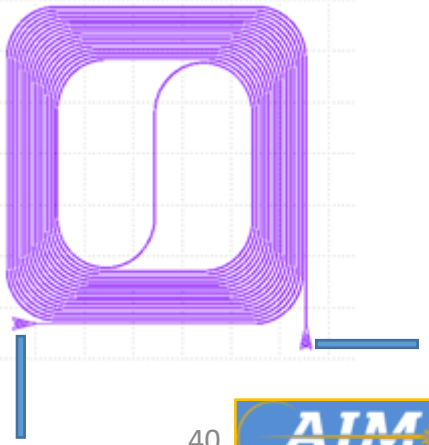




Probe Configuration: 1



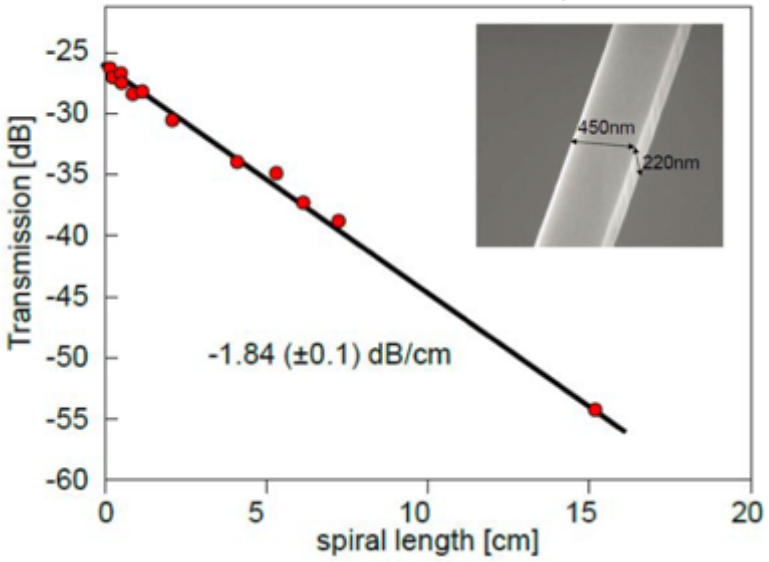
Probe Configuration: 2



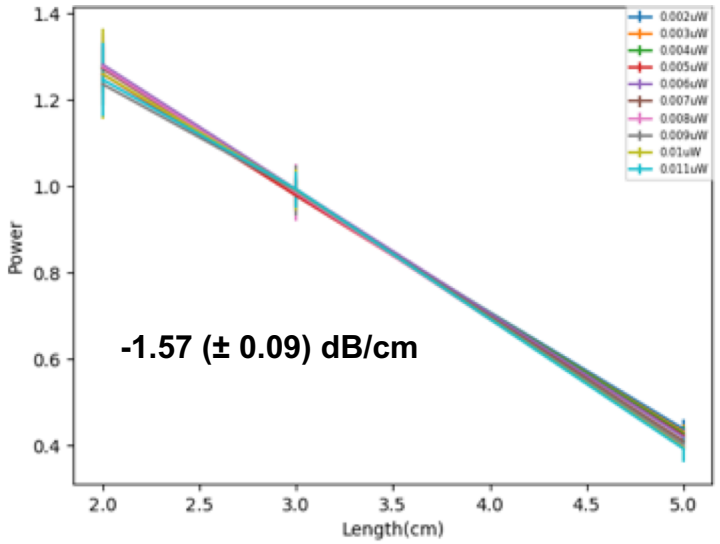
IPM: Technician Skill – "Cut-back" Loss Measurement

- **Skill Example: Data Acquisition/Collation/Documentation**
  - **Multi-power data acquisition**
  - **Collation/documentation (data port to plot & analysis)**
  - **Document for engineer team report**
- **Hands-on element for:**
  - ***Wafer-scale PIC Testing***
  - ***Chip-scale PIC Testing***

State of Art: IP waveguide

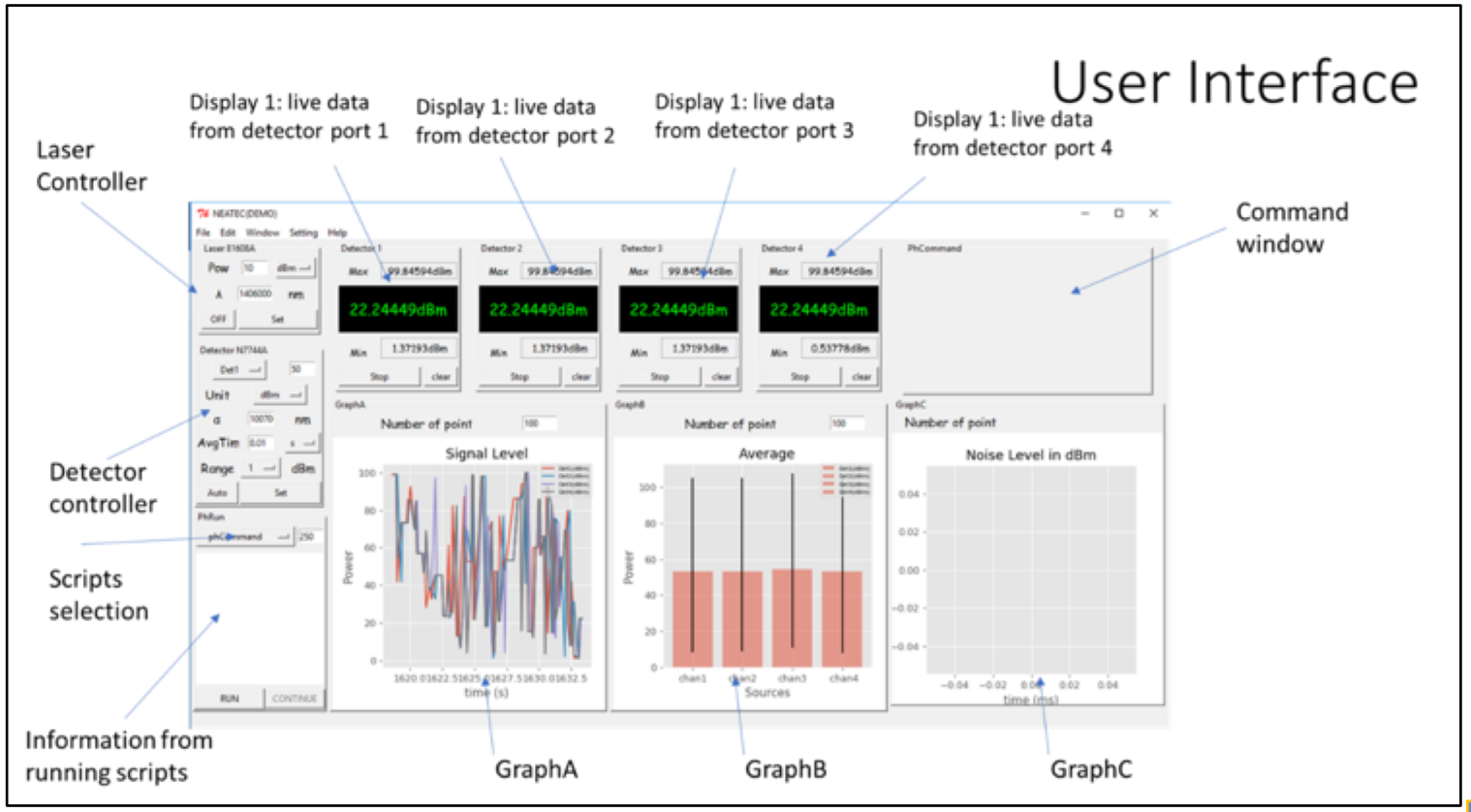


NEATEC IPM Lab Measurement:



IPM Practical Training Modules: Device Measure and Quality Control

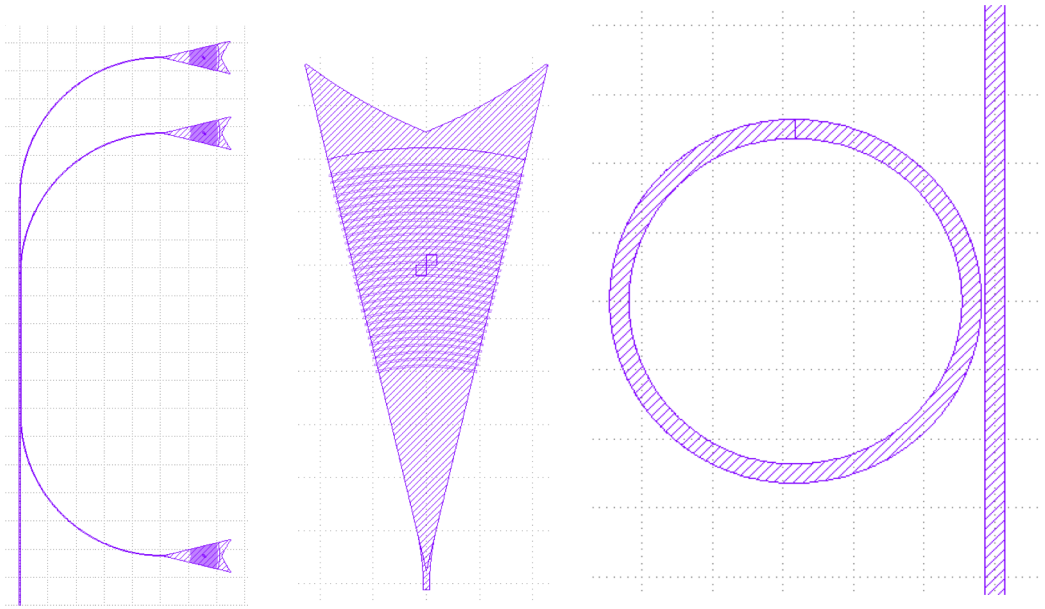
- **IPM Test Tech User Interface Development**
  - **Standard IP passive device measure (waveguides, RRs, couplers, MZIs)**
  - **Custom interface developed to support 2-year college student training**
  - **Result of Spring '18 workshop with FMCC students**

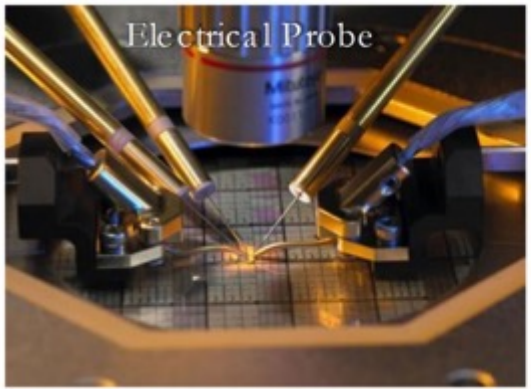


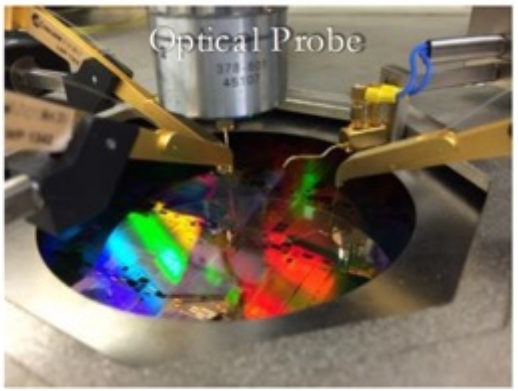
Additional Testing Protocols:

- **Technician Tasks:** **Testing protocols for basic passives/actives**

- **Passive Elements:**
  - **Couplers**
  - **Gratings**
  - **Resonators**
  - **Filters/splitters**
- **Hands-on element for:**
  - ***Wafer-scale PIC Testing***
  - ***Chip-scale PIC Testing***
- **Chipset #1:**
  - **Completed and testing protocols developed**

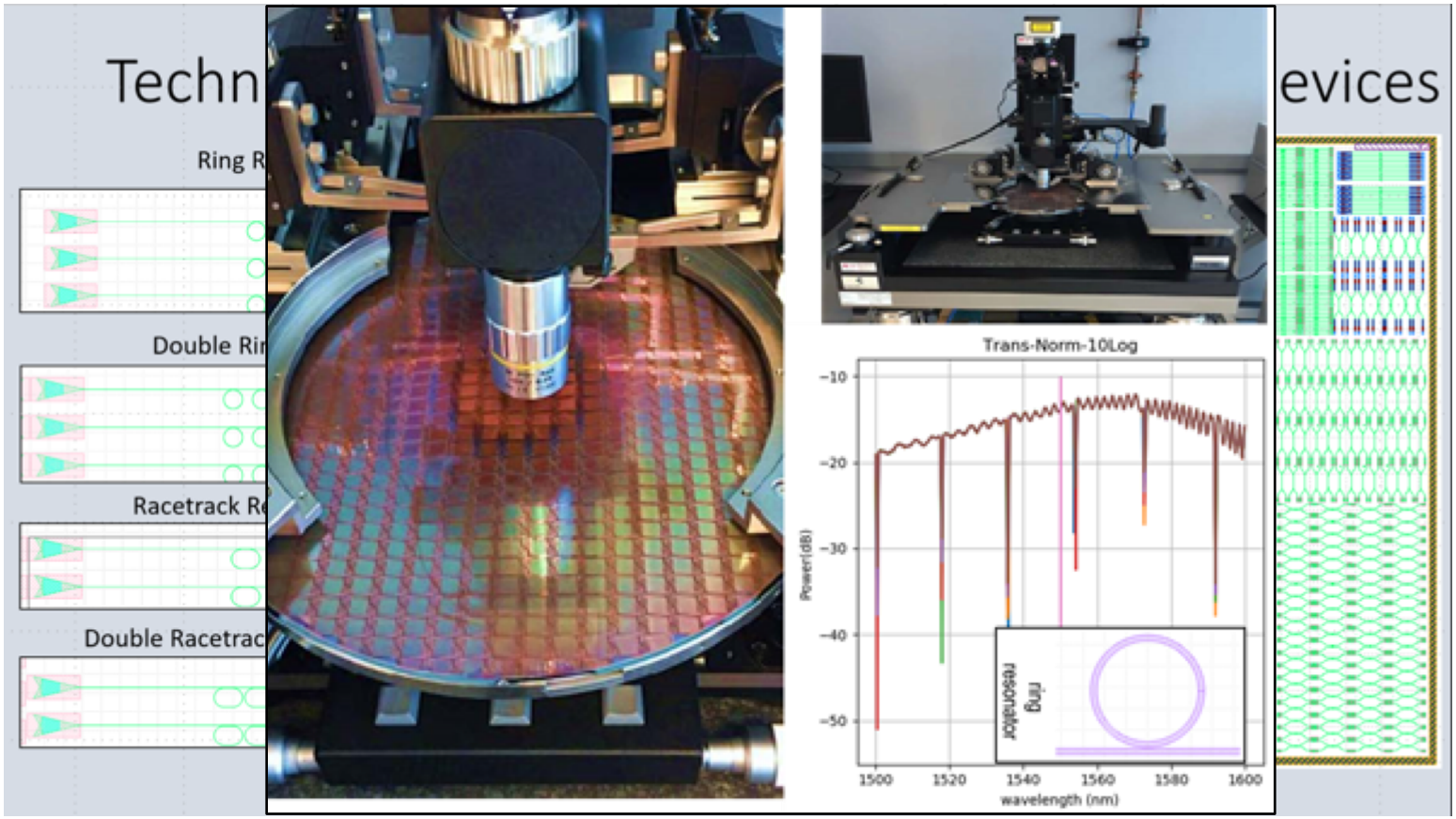






Passive and Active IP Device Fab for IP Tech Practical Training

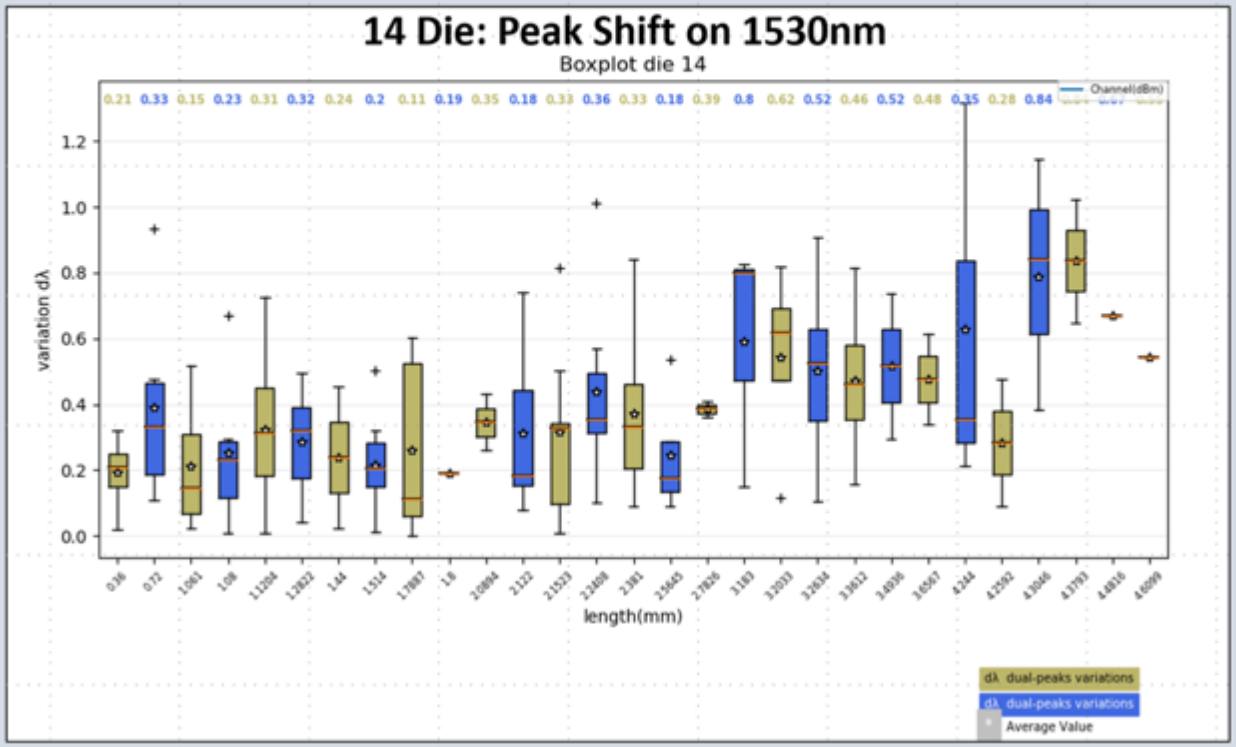
- **Devices for Technician Practical Training: Chipset #2**
  - **Standard IP passive devices (waveguides, RRs, couplers, MZIs)**
  - **Integrate onto 'dice'-able test structures for mounting into simple package**
  - **2018/2019 passive multi-project wafer (MPW) runs completed**



IPM Practical Training Modules: Device Measure and Quality Control

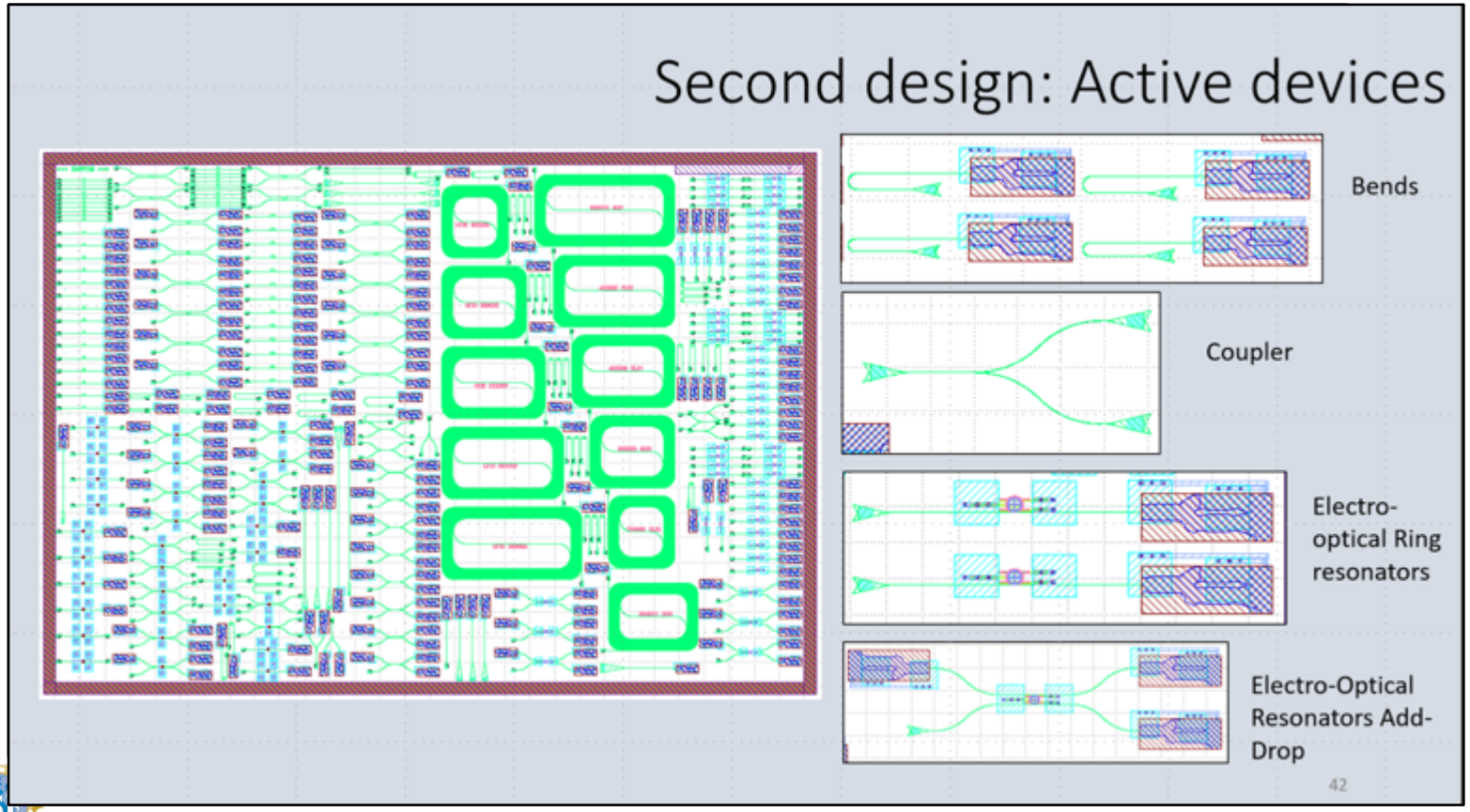
- **Within-wafer non-uniformity (WIWNU) for IP Ring Resonators**
  - **Module completed in 2018/2019**
  - **Spreadsheet based (utilized IPM Probe Station)**

IPM Practical Tech Training: Correlation Pair Analysis for RR's



Update – Passive and Active IP Device Fab for IP Tech Practical Training

- **Devices for Technician Practical Training: Chipset #3**
  - **Standard IP active devices (modulators and detectors)**
  - **Integrate onto 'dice'-able test structures for mounting into simple package**
  - **2019 one active multi-project wafer (MPW) run completed**

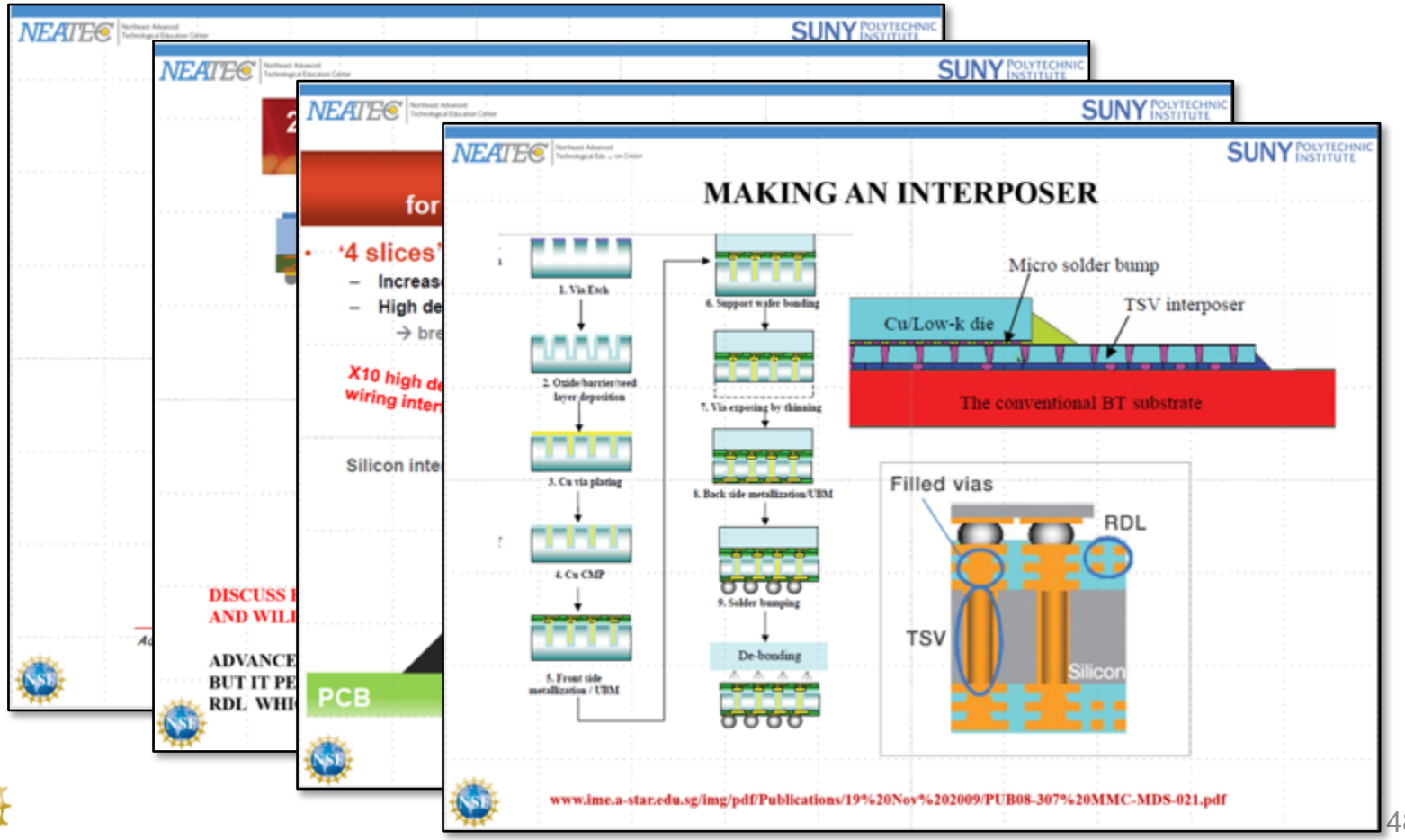


3D/2.5D Semiconductor Manufacturing Curricular Development

3D/2.5D IC Lecture Content for Tool Tech Training Modules

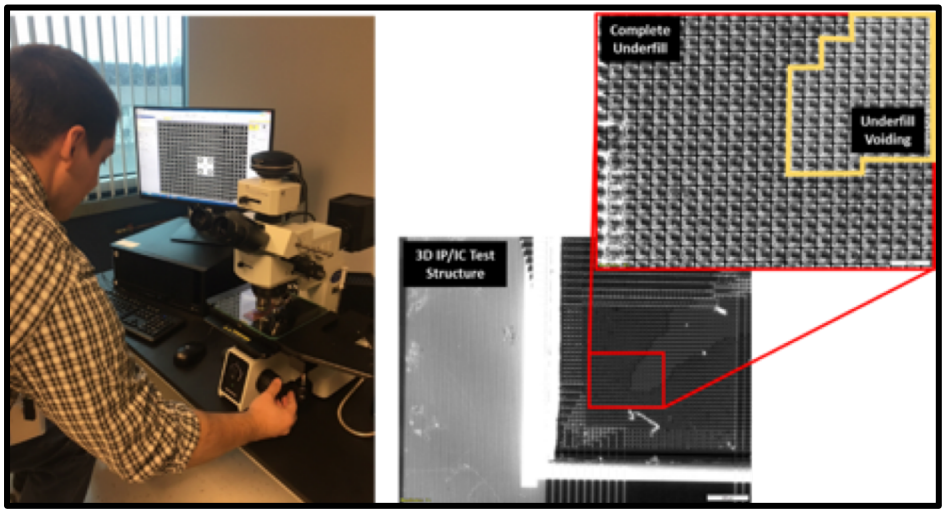
3D/2.5D Chip Stacking and Interposer Introduction for Assembly, Metrology & Tool Techs:

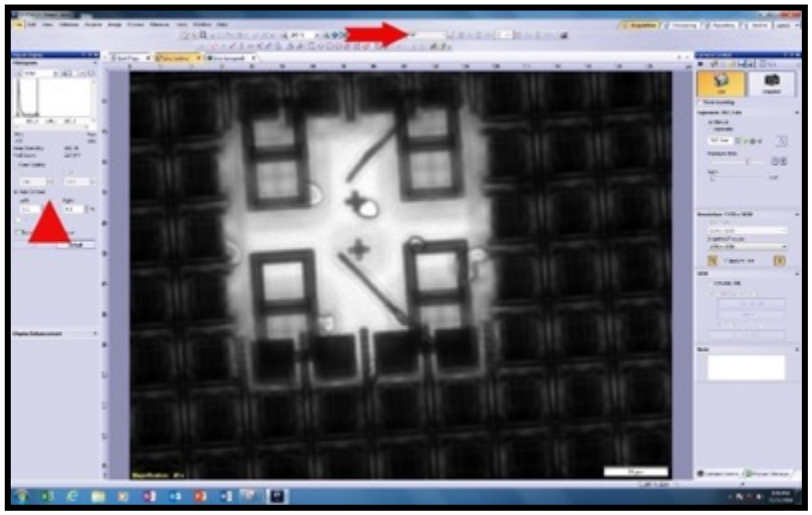
- Collaborated with CNSE faculty (Dr. Ernie Levine) on overview content for '3D/2.5D IC' fabrication
- Provide as introduction for fabrication, test, and assembly techs (for IPM)

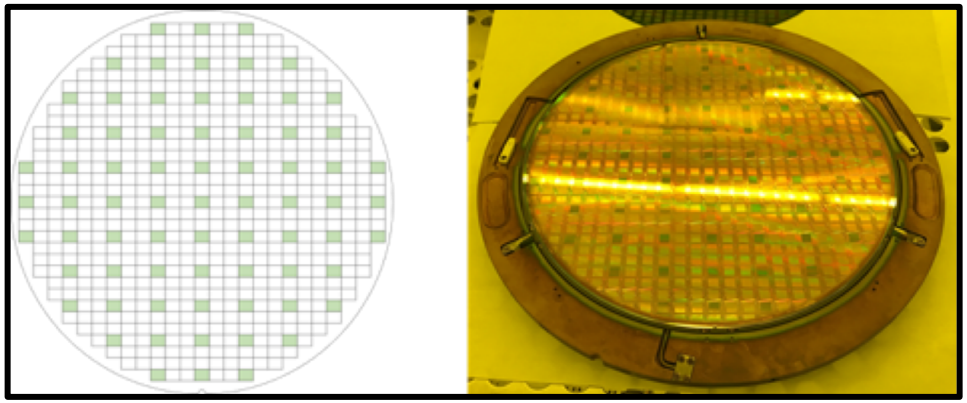


2.5D/3D IP Assembly: Practice Facility and Initial Modules

- **3D Die assembly inspection facility (IR alignment and fill inspect)**
  - **Basic module 'instruction manual' assembled**
  - **Utilized 3D die-to-wafer assembly**
  - **Die available for 2-yr college student workshops for 2019**

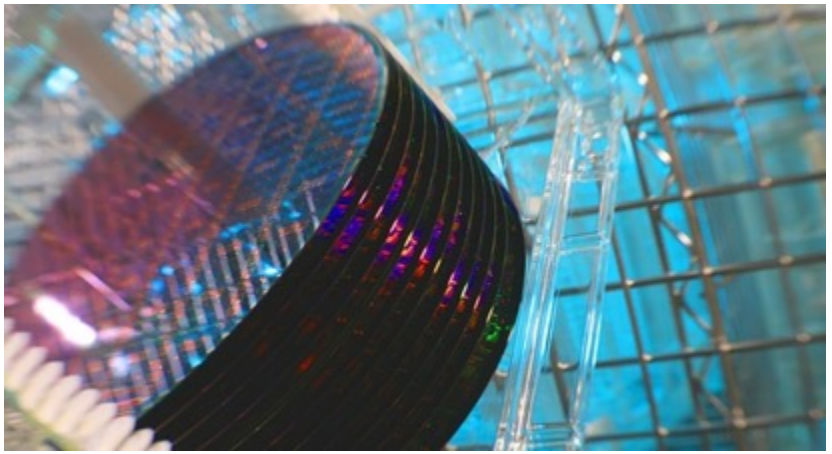


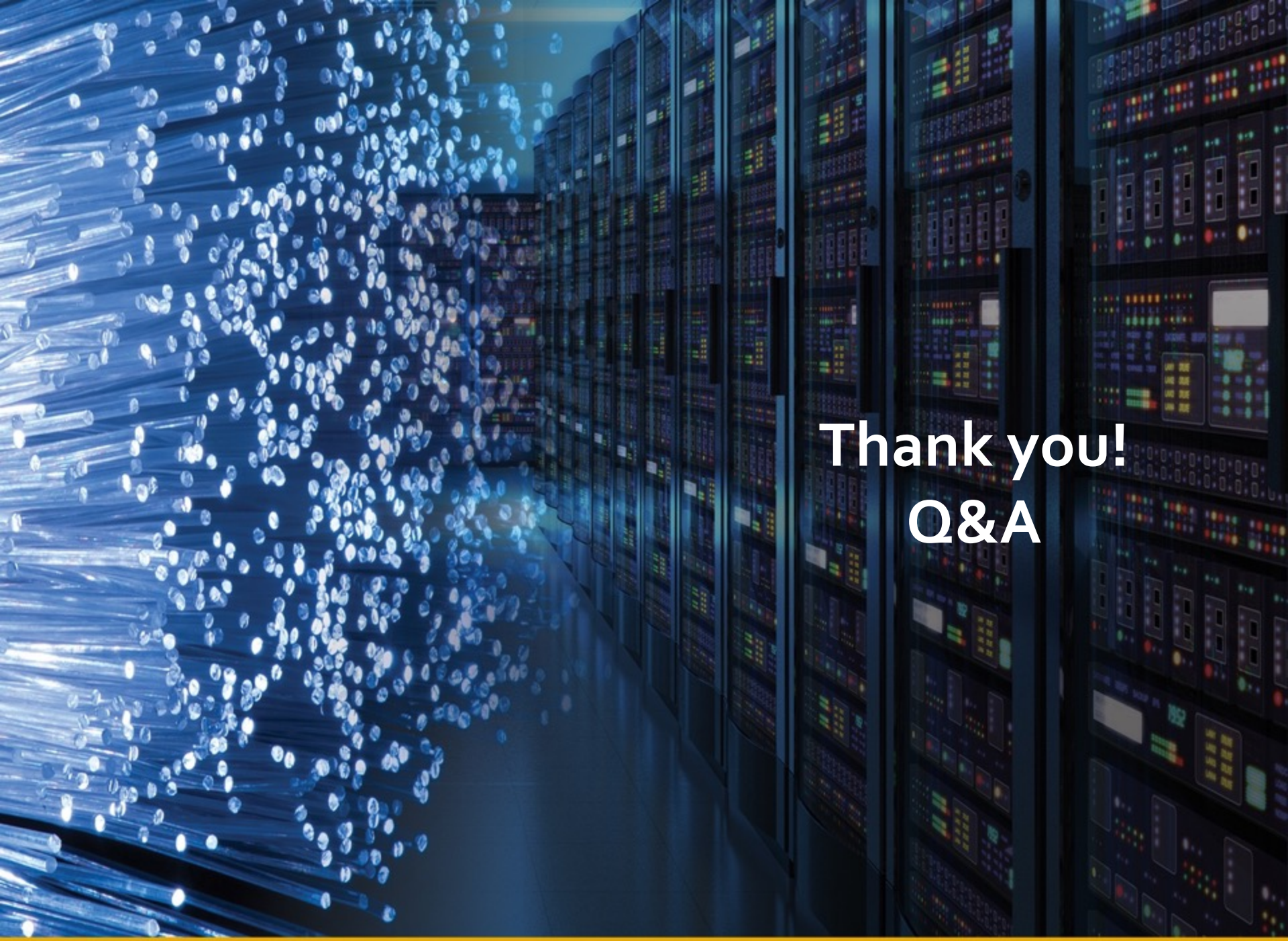




Summary and Next Steps

- Integrated Nano-Photonics is turning the corner towards HVM
- Design tools and initial foundry model in place (AIM Photonics, IMEC)
- IMP Tech Skills
  - PIC mfg skills ➔ IC fab skills
  - PIC assembly skills ➔ bridges IC & photonics
  - IP packaging/test skills photonics tech skills
- IMP Tech Education Module Development
  - Initial modules developed
  - Highly-reliant on IPM equipment
  - Need scaling model




Thank you!
Q&A

Complete our brief survey,
we want to hear from you

Join us on February 20, 2020
1 PM Eastern

NCI Southwest + NACK Network

Join us for:

Multi-Responsive Nanogels for Biosensing, Drug Delivery, and Regenerative Medicine

Hosted by: ATE Central

Date: February 20, 2020 at 10 AM MST

Register Now!